International Islamic University Chittagong
Department of Electrical and Electronic Engineering
B. Sc. Engineering in EEE
Midterm Examination, Spring 2024

Course Code: **EEE 4753** Course Title: **VLSI I**

Time: 1 hour 30 minutes Full Marks: 30

(i) Answer all the questions. The figures in the right-hand margin indicate full marks.

(ii) Course Outcomes (COs) and Bloom's Levels are mentioned in additional Columns.

Course Outcomes (COs), Program Outcomes (POs) and Bloom's Levels (BL) of the Questions	
CO	**CO Statements**
CO1	Reflect a basic understanding of IC design and fabrication technique.
CO2	Solve different problems related to MOS Device, CMOS logic circuits, and Fabrication.
CO3	Design and development of different CMOS logic circuits.

Bloom's Levels (BL) of the Questions						
Letter Symbols	**C1**	**C2**	**C3**	**C4**	**C5**	**C6**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

1. a)	"The number of transistors in a dense integrated circuit (IC) doubles about every two years". Explain/Justify the statement with necessary figures.	CO1	C4	5
1. b)	Do you think bipolar integrated circuits are superior to metal-oxide-semiconductor integrated circuits? Give your appropriate arguments in favor of your opinion.	CO2	C3	5
2. a)	Draw a CMOS inverter I. Explain its operation with transfer characteristics. II. Show different state of both transistors at different input voltages.	CO2	C4	5
2. b)	Determine the bias state for the five circuit conditions if V_{in} = 0.4 V and V_{tp} = - 0.4 **(Fig. 1)**	CO2	C5	5

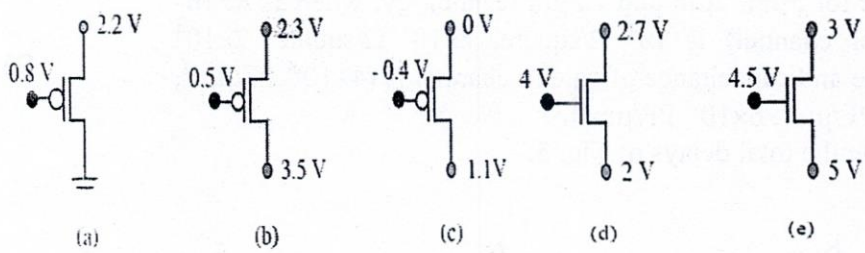

Fig. 1

OR

2) a)	Draw a nMOS inverter with nMOS enhancement type load I. Explain its operation. II. Find out the inverter ratio using typical values.	CO2	C4	5

2) b) Determine the bias state for the five circuit conditions if V_{tn} = 0.4 V and V_{tp} = - 0.4 **(Fig. 2)** CO2 C5 5

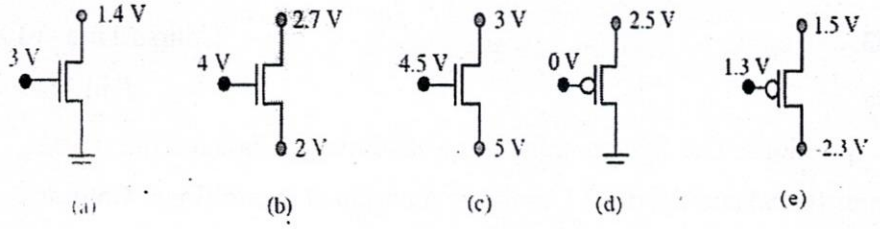

Fig. 2

3) a) **I.** "Rise time (T_r) and Fall time (T_f) are inversely proportional to threshold voltage (V_{DD})"- Is it right or wrong? Write down your logical arguments with necessary figures and expressions. CO1 C4, C5 5

II. Determine the total resistance of **Fig. 3 and Fig. 4** for 5μm, 2μm and 1.2μm technology, whereas *Rs* (n-transistor channel) is 10^4 Ω/square, 2×10^4 Ω/square, 2×10^4 Ω/square, and *Rs* (p-transistor channel) is 2.5×10^4 Ω/square, 4.5×10^4 Ω/square, 4.5×10^4 Ω/square.

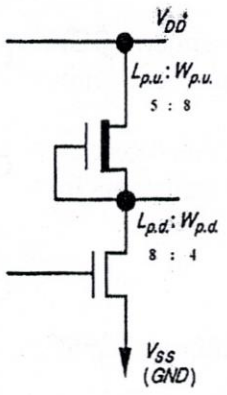

Fig. 3 nMOS Inverter

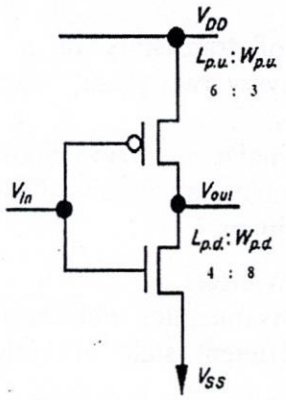

Fig. 4 CMOS Inverter

3) b) **I.** What is the delay unit of MOS circuits? Determine the delay unit of τ for 5μm, 2μm and 1.2μm technology, whereas *Rs* (n-transistor channel) is 10^4 Ω/square, 2×10^4 Ω/square, 2×10^4 Ω/square and capacitance of gate to channel is (4×10^{-4} PF/μm^2, 8×10^{-4} PF/μm^2, 6×10^{-4} PF/μm^2). CO2 C2, C3 5

II. Calculate the total delays of **Fig. 5.**

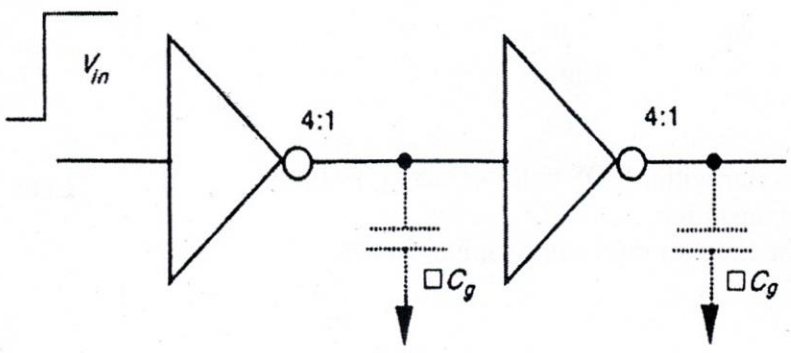

Fig. 5 Cascaded nMOS inverters