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Department of Computer and Communication Engineering

Semester End Examination

Program: **B.Sc. (Engg.)**
Course Code: **CCE -3509**
Total Marks: **50**

Semester: **Spring 2022**
Course Title: **Computer Architecture**
Time: **2 Hours 30 Minutes**
Date: 15/12/2022

(i) Answer all the questions. The figures in the right-hand margin indicate full marks.
(ii) Course Learning Outcomes (CLOs) and Bloom's Levels are mentioned in additional Columns.

Course Learning Outcomes (CLOs) of the Questions	
CLO1	Understand the Overview, Computer System, Arithmetic and logic, Central processing unit and parallel Organization.
CLO2	Understand the Computer and Processor Design, Hazards; Exceptions; external and internal memory Pipeline and multiple processor systems.
CLO3	Develop and design an instruction set architecture and subsystems of central processing unit.

Bloom's Levels of the Questions						
Letter Symbols	**R**	**U**	**Ap**	**An**	**E**	**C**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

PART-A

[Answer two questions from the following]

Q1.	**a)**	What is the purpose of **interrupts**? Differentiate between **Maskable** and **Non-maskable** interrupts.	**CLO1**	**R, An**	**4**
	b)	Discuss briefly establishment of priority of simultaneous interrupts using **Daisy Chaining priority interrupt** with proper diagram.	**CLO1**	**Ap**	**6**
Q2.	**a)**	State the **Limitations** of Programmed I/O.	**CLO1**	**E**	**3**
	b)	Explain the **operation of DMA** using a block diagram. Give an example application of **DMA data transfer**.	**CLO1**	**An**	**7**
		OR			
Q2.	**a)**	Enumerate the characteristics of **RISC** architectures.	**CLO3**	**U**	**3**
	b)	**Micro-programmed control is not suitable for RISC architecture** - Justify the validity or otherwise of this statement.	**CLO3**	**E**	**7**

PART-B

[Answer three questions from the following]

Q3.	**a)**	What do you mean by **pipelining**? How is **instruction pipelining** different from **arithmetic pipelining**?	**CLO2**	**U, An**	**5**
	b)	Explain **Asynchronous pipeline** model with proper diagram.	**CLO2**	**An**	**5**

Q4.	**a)**	Compare **Instruction-Level** Parallelism and **Machine** Parallelism.	**CLO2**	**An**	**3**
	b)	With reference to pipelining, what is **data hazard**? Explain briefly about possible data hazards.	**CLO2**	**Ap**	**7**
Q5.	**a)**	Write a short note on **Branch Prediction**.	**CLO2**	**U**	**3**
	b)	What is the **cache coherence** problem in a multiprocessor? How can the problem be resolved? Briefly explain the **important schemes** available for this.	**CLO2**	**R, An**	**7**

OR

Q5.	**a)**	Why RISC architecture is also called **load/store** architecture?	**CLO3**	**An**	**3**
	b)	What do you mean by Instruction Level Parallelism? Write the important approaches available to exploit instruction level parallelism.	**CLO2**	**R, An**	**7**

***** Good Luck *****