

**International Islamic University Chittagong**  
**Department of Electrical and Electronic Engineering**

**Final Assignment Test Autumn-2020**

Course Code: **EEE-2301**

Time: **5 hours** (Writing- **4 hours 30 minutes** + **30 minutes** submission time)

Program: B.Sc. Engg. (EEE)

Course Title: **Electronics-I**

Full Marks: **50** (Written 30 + Viva/Viva-Quiz-20)

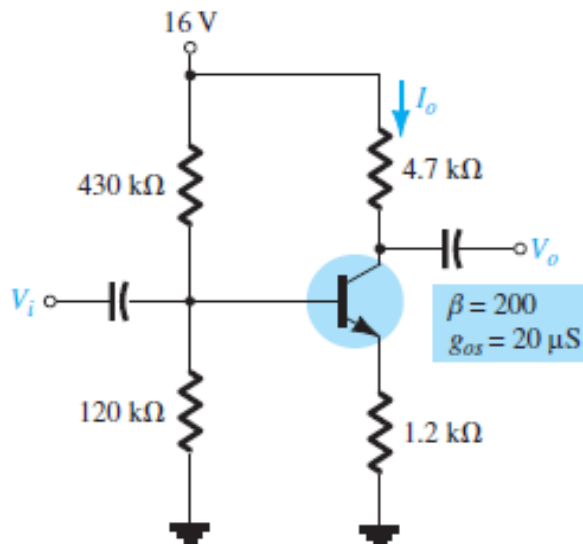
[Answer each of the questions (1-5) from the followings; Figures in the right margin indicate full marks.]

Don't blindly copy any answer from book/internet/friend. There is serious penalty for plagiarism. A straight zero will be given for the cause. Please write from your own understanding.

Question Distribution Procedure	
Last Two digits of Student ID	SET Number
Even , Even	SET-A
Even , Odd	SET-B
Odd , Even	SET-C
Odd , Odd	SET-D

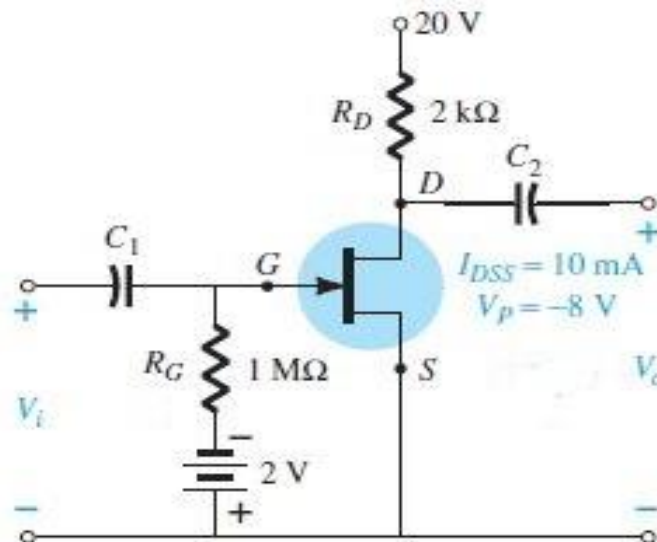
**SET-D**

- 1(b). Evaluate the equations for voltage gain, current gain, input impedance, and output impedance for a BJT using low-frequency h-parameter model for CB configuration. CO3 Ev 03
- 1(c). For the network of “Fig. 1”, Determine CO2 Ev 03
- a.  $r_e$ .
  - c.  $Z_i$  and  $Z_o$ .
  - d.  $A_v$ .



“Fig. 1” BJT voltage-divider biasing circuit.

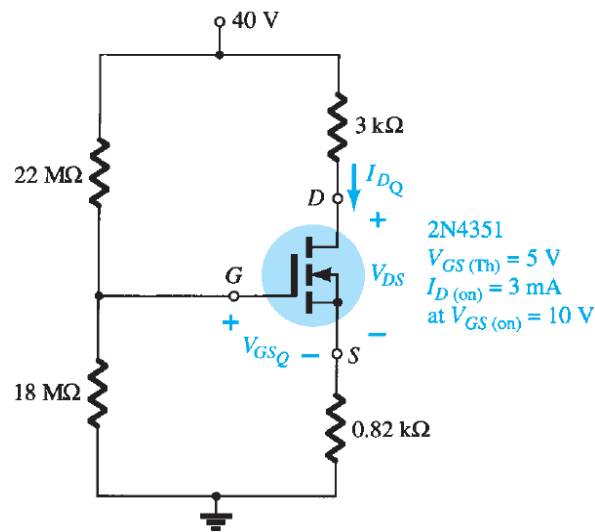
- 2(a). Justify the answer, why frequency response of RC coupled amplifier decreases at high frequencies? **CO1 Ev 02**
- 2(b). Show that the magnitude of single-ended voltage gain at either collector of a differential amplifier is  $A_v = \frac{R_c}{2r_e}$ ; where the symbols have their usual meaning. **CO3 Ap 03**
- 2(c). A multistage amplifier consists of three stages; the voltage gain of the stages is 60,100 and 160. Calculate the overall gain. **CO2 Ev 01**
- 3(a). What do you understand by pinch off? When it occurs in a JFET? Is there any effect of  $V_{GS}$  on pinch off? **CO1 An 01**
- 3(b). Design a self-bias network using a JFET transistor with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -6 \text{ V}$  to have a  $Q$ -point at  $I_{DQ} = 4 \text{ mA}$  using a supply of 14 V. Assume that  $R_D = 3R_S$  and use standard values. **CO3 Cr 03**
- 3(c). The network shown in “Fig. 2” has an operating point at  $V_{GSQ} = -2 \text{ V}$  and  $I_{DQ} = 5.625 \text{ mA}$ . Determine  $g_m$ ,  $Z_i$ ,  $Z_o$ , and  $A_v$ . Consider the output admittance as  $40 \mu\text{S}$ . **CO2 Ev 02**



“Fig. 2” n-channel (Fixed biased) JFET circuit.

- 4(a). Explain in your own words why the application of a positive voltage to the gate of an  $n$ -channel depletion-type MOSFET will result in a drain current exceeding  $I_{DSS}$ . **CO1 An 02**
- 4(b). What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET? In your own words, briefly describe the basic operation of an enhancement-type MOSFET. **CO1 An 04**

- 5(a). Consider the enhancement MOSFET of “Fig. 3”. Determine the levels of  $V_{DSQ}$  and  $I_{DQ}$ . CO2 Ev 02



“Fig. 3” n-channel enhancement MOSFET.

- 5(b). Determine the operation of UJT relaxation oscillator and  $R_1$  value from the conditions for turn-on and turn-off. CO2 Ev 02
- 5(c). Show that CMOS acts as an inverter. CO1 Ap 02
6. Viva-Quiz: The time of viva-quiz will be declared in google classroom. CO1 20

Prepared by,

Name: Md. Lokman Hossain  
 Designation: Lecturer  
 Department: EEE