DESIGNING AN IC LAYOUT FOR BANGLA ALPHABET CHARACTER

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DECLARATION

We hereby declare that the work have been done by myself and no portion of the work contained in this thesis has been submitted in support of any application for any other degree or qualification of this or any other university or institute of learning.

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ABSTRACT

This thesis discusses the design of an integrated circuit layout for Bangla Alphabet character. Due to concerns of cost, power loss and design complexity the IC based Bangla Alphabet character display become more popular over the other method. Such as microcontroller based method. There are a little work done on the field of IC based Bangla Alphabet character technology. In this thesis we have tried to propose an IC which is capable to make all the Bangla alphabet character. In order to produce the layout, the basic knowledge of fabrication process and IC design rule are expounded. The complete layout of the IC was designed based on its schematic circuit, diagram which consists of NOT gate, 5-input AND gate, 2-input and 3-input and 5-input OR gate. The layout has undergone design rule checker by MICROWIND. Both layout and schematic circuit of the IC were than simulated through MICROWIND and DSCH to ensure they were identical. The both simulated output of IC should be essentially identical and should match the theoretical results. All Bangla vowel and consonant can be characterized through our proposed IC.

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CHAPTER 1: INTRODUCTION

1.1 Introduction

Electronic devices have been widely used in many different fields and the size of these devices has been gradually reduced. An example of this is the mobile phone which is made smaller to enhance user's mobility and usage time. These are the contribution of integrated circuit (IC) technology. With this technology, the modern devices have been reduced to convenient sizes. Besides that, mass production of IC has lowered the cost of production and made most electronic devices affordable. Today, an IC is smaller than a coin and can hold millions of transistors. Hence, further research in the design of IC is important to enhance the production of a more efficient and viable IC. The main purpose of this analysis is to design an IC layout of a 26-segments display by Electric VLSI Design System. It also helps to boost the electronic field of our country. Besides this we have tried to make it more users friendly. If we have got our desired success then this IC can help our print industry in near future.

1.2 Objectives

The objective of the thesis are given below

- To design an IC layout for Bangla Alphabet Character by Electrical VLSI design System.
- To develop statistical shape based technology so that it can enhance its flexibility and life time.
- To test and verify the applicability of the designed IC.
- To develop an IC based technology to reduce the cost and lost.

The main objective of this analysis is design an IC for Bangla Alphabet character. The other purpose of this analysis is to enhance flexibility, life time of the device. Then the print media

and printing industry can work in more comfortable environment and the working method will become more convenient and faster than previous.

1.3 Motivations

At first as a nation we are Bengali. So from the very beginning we have wanted to do something for our homeland. Accurate display of Bangla alphabet character is a challenge since the bangla alphabet are more gnarled such as (□,□□) and complex than any other alphabet like English alphabet. Besides this there is a challenge to make the technology more convenient user friendly and cost effective. Many methods have been developed in overcoming these difficulties.

Microcontroller based numerical display: Some microcontroller based works such as (Display unit for Bangla alphabet character)[] only work with Bangla numerical numbers such as (□,□,□,□).This method has some difficulties with Bangla Alphabet Character.

Proceeding on this way we have found that very negligible number of works had been done on this field. In that analysis we have found that there were difficulties and limitation for the user. We have tried to overcome those limitations through our endeavor. In those analyses they had mostly worked on display, but they never tried to give any solution of the problem through designing of an IC. This inspired us more. Here we have tried to design an IC which makes the Bangla Alphabet technology more compact faster and user friendly.

1.4 Thesis Outlines

Chapter 1 serves to provide introduction to IC based technology for Bangla Alphabet character along with motivation, objective, of the work undertaken in this thesis.

Chapter 2 provides information about background of this thesis. It provides information about the different components that necessary for work and about their behavior.

Chapter 3 provides information about the methodology of the work undertaken in this thesis.

Chapter 4 provides information about the practical data of the thesis. It describes the calculation procedure of the thesis.

Chapter 5 provides the overall summary of the methodology, achievements and results of the thesis. In addition, it discusses the shortcomings of the proposed technique and provides suggestions for future work.

1.5 Summary

In this chapter we have discussed about some basic points. Here we have disclosed our point of inspiration.From what point and from where we get our motivation. From this chapter viewer can realize about the content of different chapter.

CHAPTER 2: BACKGROUND STUDY

2.1 Introduction

When we get an idea about designing of an IC that can produce Bangla alphabet we started to think how to design our desired IC. Then we found that for the designing of IC it was very much necessary to understand the construction behavior of AND gate NOT gate OR gate decoder etc. Then we started to analyze the construction truth table, operation of the gate one by one. We have also analyzed which type of MOS will be better to design our desired gate. But another point to determine what will be the segment number of the display. Since the output of our IC is completely related with the display that's why we have to analyze about display and the segment number of display.

2.2 Component Description

Here in this section we will discuss about different types of gates and displays. Here we will explain their operation mechanism logic diagram and truth table.

1. AND Gate .

2. OR Gate.

3. NOT Gate.

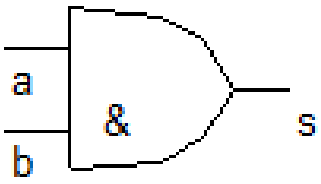
4. Decoder.

5. 26-Segment Display.

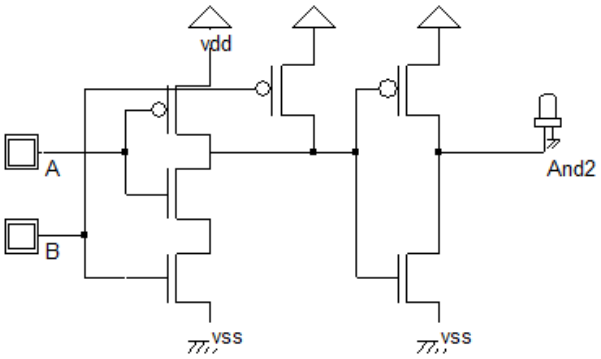
6. Dot matrix Display.

2.2.1 AND Gate

The output s is true if input a AND input b are both true: Y = A AND B. An AND gate can have two or more inputs, its output is true if all inputs are true. Here true means high. Fig.2.1 (a) And Fig.2.1 (b) shows the schematic diagram and layout design of a 2 input AND gate. From the time diagram in Fig 2.2 we have checked the performance of our designed AND gate. We have done frequency domain analysis to check its stability which has showed in Fig 2.3.



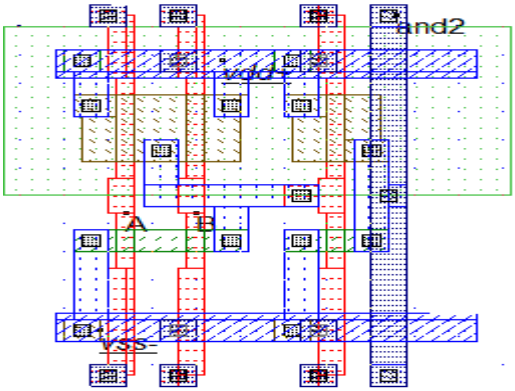
(a)



(b)

Table 2.1: Truth table of AND gate

Input		Output
A	B	F=A.B
0	0	0
0	1	0
1	0	0
1	1	0



(c)

Fig. 2.1: AND gate (a) Logicl circuit (b) Schematic diagram (c) Layout

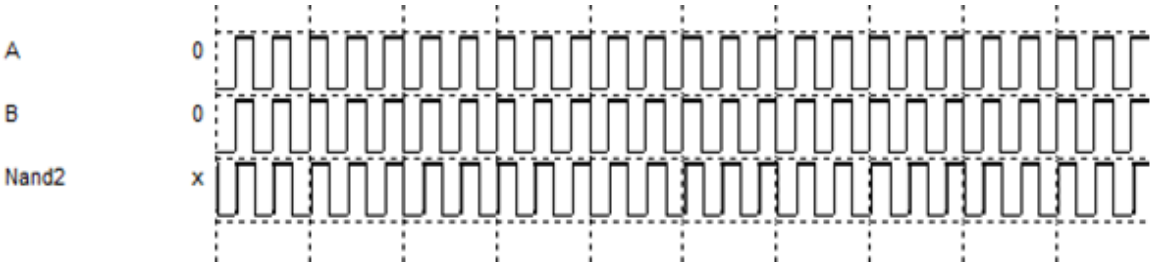


Fig.2.2: Timing diagram of AND gate.

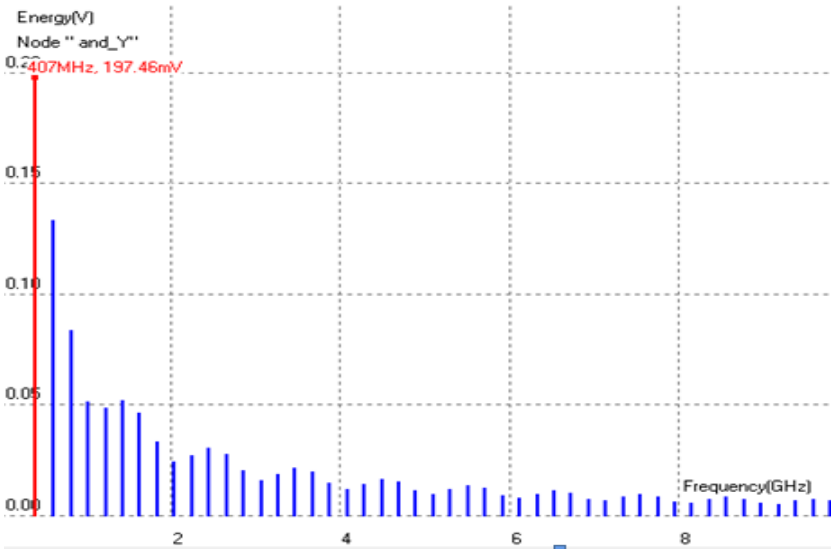


Fig.2.3: FFT curve

2.2.1.1 Verilog file, VHDL code for AND gate

```
USER SYMBOL by DSCH 2.7f
DATE 5/5/2015 11:35:26 AM
SYM  #and2Cmos
BB(0,0,40,30)
TITLE 10 -2  #and2Cmos
MODEL 6000
REC(5,5,30,20)
PIN(0,10,0.00,0.00)B
PIN(0,20,0.00,0.00)A
PIN(40,10,2.00,1.00)And2
LIG(0,10,5,10)
LIG(0,20,5,20)
LIG(35,10,40,10)
LIG(5,5,5,25)
LIG(5,5,35,5)
LIG(35,5,35,25)
LIG(35,25,5,25)
VLG module and2Cmos( B,A,And2);
VLG  input B,A;
VLG  output And2;
VLG  pmos #(114) pmos(And2,vdd,w2); // 2.0u 0.12u
VLG  pmos #(128) pmos(w2,vdd,B); // 2.0u 0.12u
VLG  nmos #(114) nmos(And2,vss,w2); // 1.0u 0.12u
VLG  pmos #(128) pmos(w2,vdd,A); // 2.0u 0.12u
VLG  nmos #(128) nmos(w2,w5,A); // 1.0u 0.12u
VLG  nmos #(107) nmos(w5,vss,B); // 1.0u 0.12u
VLG endmodule
FSYM
```

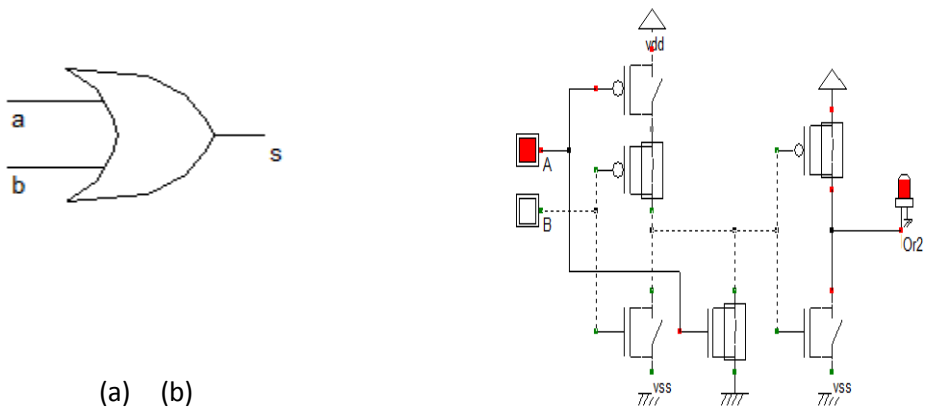
VHDL Source Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity andgate is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
y : out STD_LOGIC);
end orgate;
architecture arch_andgate of andgate is
begin
y<= a and b;
end arch_andgate;
```

2.2.2 OR Gate

The output Y is true if input A OR input B is true (or both of them are true): Y = A OR B. An OR gate can have two or more inputs, its output is true if at least one input is true. Fig 2.4 (a) and (b) show the logic circuit and schematic diagram and Fig 2.5 shows the layout of OR gate. From the time diagram in Fig 2.6 we have checked the performance of our designed OR gate. We have done frequency domain analysis to check its stability which has showed in Fig 2.7.



(a) (b)

Fig.2.4: OR gate (a) Logic circuit (b) Schematic diagram.

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Table 2.2: Truth table of OR gate

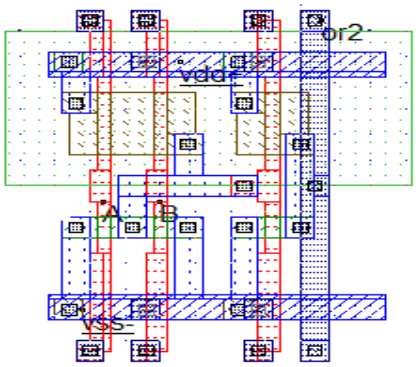


Fig.2.5: Layout of OR gate

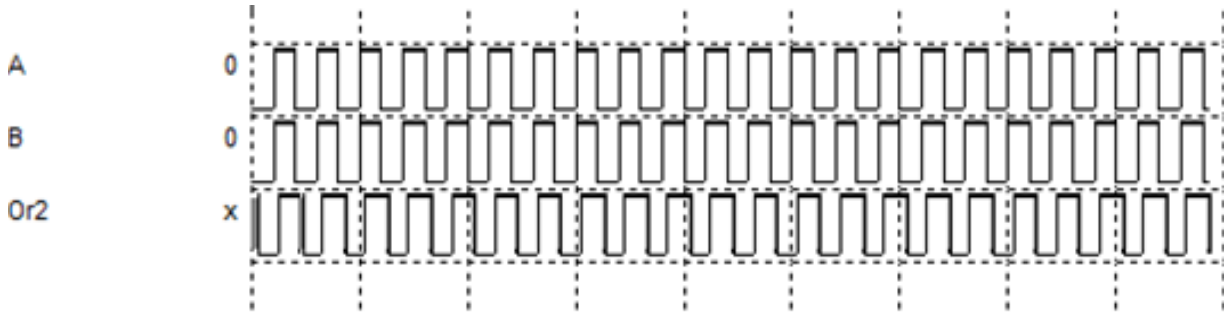


Fig.2.6: Timing diagram of OR gate.

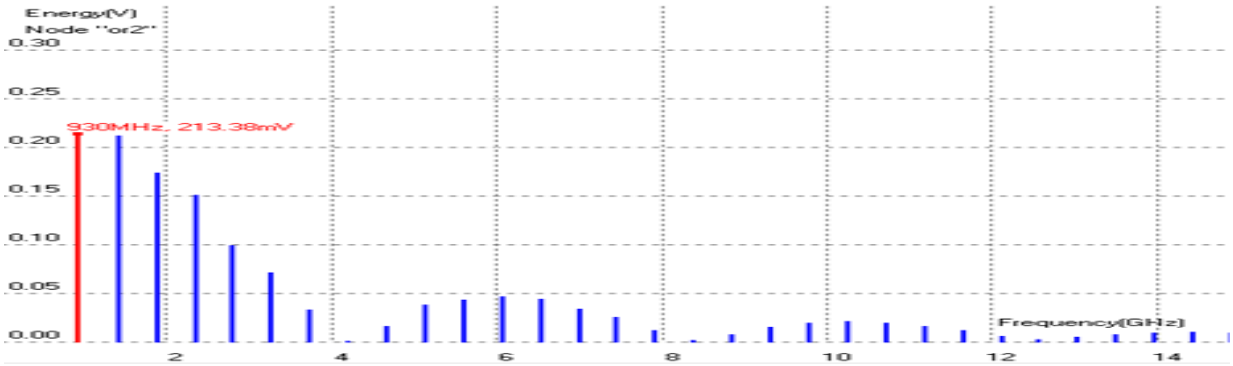


Fig.2.7: FFT curve

2.2.2.2 Verilog file and VHDL code for OR gate

```
USER SYMBOL by DSCH 2.7f
DATE 5/5/2015 11:32:14 AM
SYM  #or2Cmos
BB(0,0,40,30)
TITLE 10 -2  #or2Cmos
MODEL 6000
REC(5,5,30,20)
PIN(0,20,0.00,0.00)A
PIN(0,10,0.00,0.00)B
PIN(40,10,2.00,1.00)Or2
LIG(0,20,5,20)
LIG(0,10,5,10)
LIG(35,10,40,10)
```

```
LIG(5,5,5,25)
LIG(5,5,35,5)
LIG(35,5,35,25)
LIG(35,25,5,25)
VLG module or2Cmos( A,B,Or2);
VLG  input A,B;
VLG  output Or2;
VLG  nmos #(114) nmos(Or2,vss,w2); // 1.0u 0.12u
VLG  pmos #(114) pmos(Or2,vdd,w2); // 2.0u 0.12u
VLG  pmos #(128) pmos(w2,w4,B); // 2.0u 0.12u
VLG  nmos #(128) nmos(w2,vss,A); // 1.0u 0.12u
VLG  nmos #(128) nmos(w2,vss,B); // 1.0u 0.12u
VLG  pmos #(107) pmos(w4,vdd,A); // 2.0u 0.12u
VLG endmodule
FSYM
```

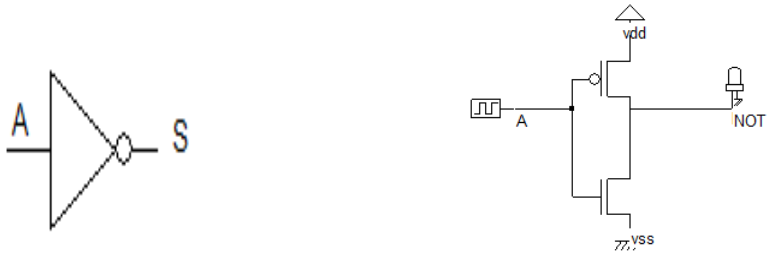
VHDL Source Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity orgate is
Port ( a : in STD_LOGIC;
b : in STD_LOGIC;
y : out STD_LOGIC);
end orgate;
architecture arch_orgate of orgate is
begin
y<= a and b;
end arch_orgate;
```

2.2.3 NOT Gate

The output Q is true when the input A is NOT true; the output is he inverse of the input: **Y = NOT A.** A NOT gate can only have one input. A NOT gate is also called an inverter. Fig 2.8 (a) and (b) shows the logic circuit and schematic diagram and Fig 2.9 shows the layout of OR gate. From

the time diagram in Fig 2.10 we have checked the performance of our designed OR gate. We have done frequency domain analysis to check its stability which has showed in Fig 2.11.



(a) (b)

Fig.2.8: NOT gate (a) Logic circuit (b) Schematic diagram

Table 2.3: Truth table of NOT gate

Input	Output
A	F=A’
0	1
0	1
1	0
1	0

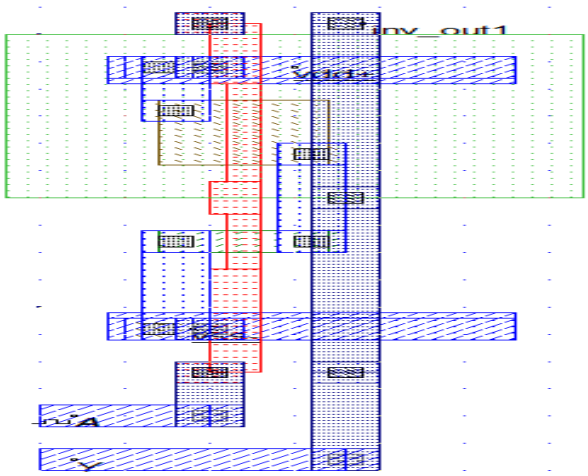


Fig.2.9: Layout of OR gate

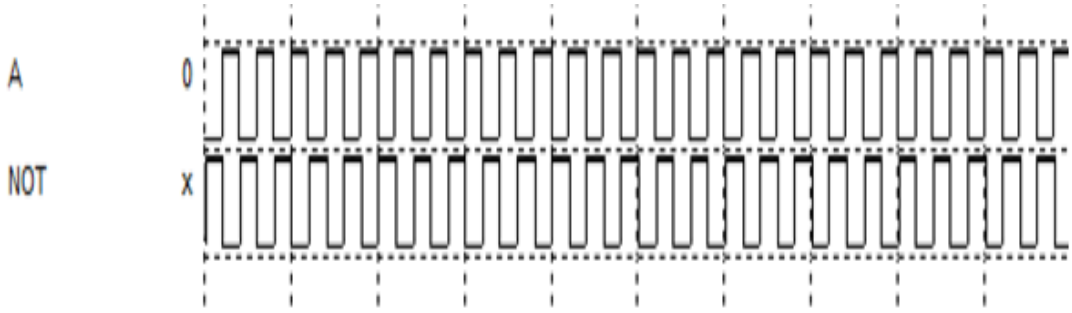


Fig.2.10: Timing diagram of NOT gate

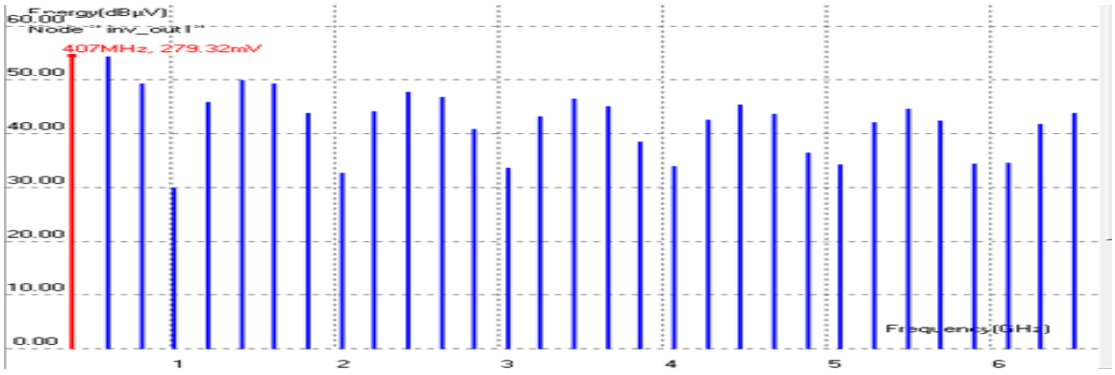


Fig.2.11: FFT curve

2.2.3.1 Verilog file and VHDL code for NOT gate

```
USER SYMBOL by DSCH 2.7f
DATE 5/5/2015 11:40:15 AM
SYM  #Not
BB(0,0,40,20)
TITLE 10 -2  #Not
MODEL 6000
REC(5,5,30,10)
PIN(0,10,0.00,0.00)A
PIN(40,10,2.00,1.00)Not
LIG(0,10,5,10)
LIG(35,10,40,10)
LIG(5,5,5,15)
LIG(5,5,35,5)
LIG(35,5,35,15)
LIG(35,15,5,15)
VLG module Not( A,Not);
VLG  input A;
VLG  output Not;
VLG  nmos #(114) nmos(Not,vss,A); // 1.0u 0.12u
VLG  pmos #(114) pmos(Not,vdd,A); // 2.0u 0.12u
VLG endmodule
FSYM
```

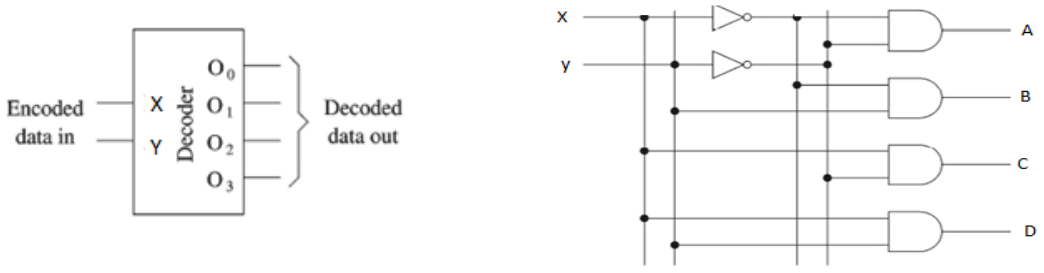
VHDL Source Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
```

```
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity notgate is
Port ( a : in STD_LOGIC;
y : out STD_LOGIC);
end notgate;
architecture arch_notgate of notgate is
begin
y<= not a;
end arch_notgate;
```

2.2.4 Decoder

Decoder selects one out of N Inputs. Fig 2.12 (a) and (b) shows the symbol and schematic diagram and Fig 2.13 shows the layout of OR gate. From the time diagram in Fig 2.14 we have checked the performance of our designed OR gate.



(a) **(b)**

Fig.2.12: Symbol (a) and schematic diagram (b) of Decoder

Table2.4: Truth table of decoder

Input		Output
x	**y**	
0	**0**	**A**
0	**1**	**B**

1	0	C
1	1	D

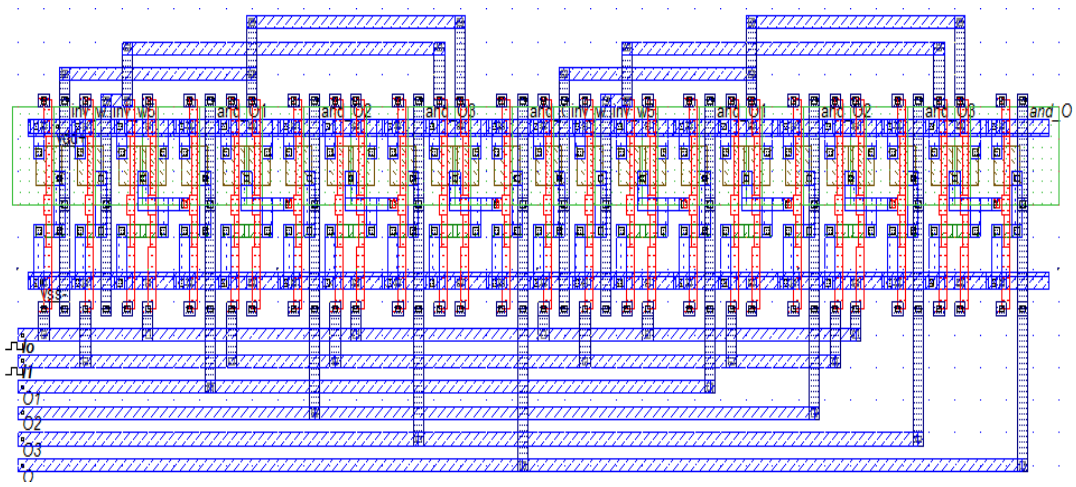


Fig.2.13: Layout of Decoder

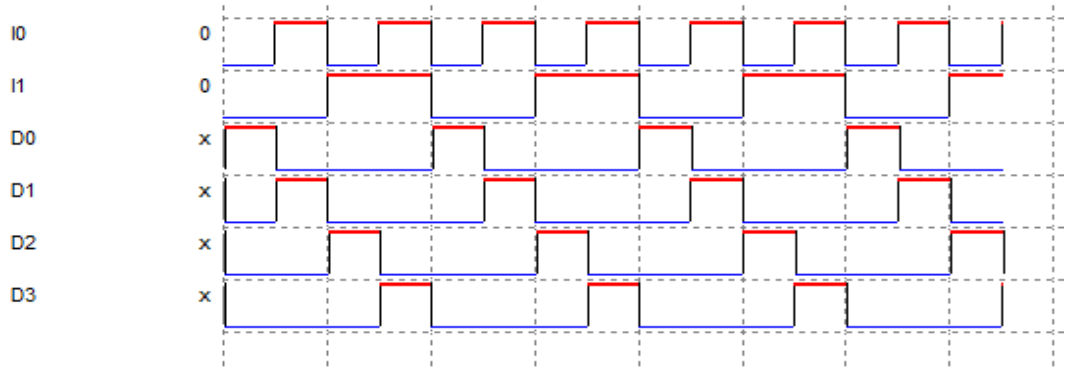


Fig.2.14: Timing diagram of decoder

2.2.4.1 Verilog file

```
// DSCH 2.7f
// 5/5/2015 1:03:29 AM
// C:\Users\mamun\Desktop\adder rab.sch
module adder rab( I0,I1,D0,D1,D2,D3);
```

```
 input I0,I1;
 output D0,D1,D2,D3;
 not #(17) inv(w2,I0);
 not #(17) inv(w4,I1);
 and #(16) and(D0,w4,w2);
 and #(16) and(D1,w4,I0);
 and #(16) and(D2,I1,w2);
 and #(16) and(D3,I0,I1);
endmodule

// Simulation parameters in Verilog Format
always
#1000 I0=~I0;
#2000 I1=~I1
;
// Simulation parameters
// I0 CLK 10.000 10.000
// I1 CLK 20.000 20.000
```

2.2.5 Display

Here, we have used 26-segments display (shown in Figure 2.16). All Bangla characters vowel and consonants can be characterized by using this26-segments display. As there can be at least vowels (12) and consonants (39) and some special symbols to be displayed, 6-bits input are used to represent each character. After analyzing which segments will be activated for which character, appropriate logic function and circuits have been derived in order to display each Bangla character.

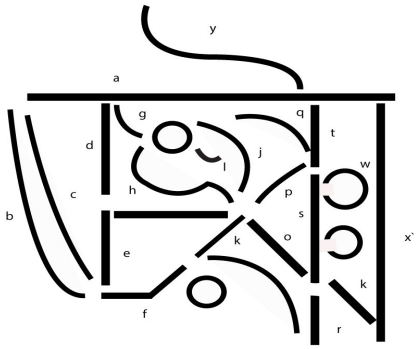


Fig. 2.15: Segmentation of display

2.2.6 Dot matrix

A dot matrix is a 2-dimensional patterned array, used to represent characters, symbols and images. Every type of modern technology uses dot matrices for display of information, including cell phones, televisions and printers. Now a dot matrix display is a display device used to display information on machines, clocks, railway departure indicators and many other devices requiring a simple display device of limited resolution. The display consists of a dot matrix of lights.

2.3 Literature review

There are different technologies to construct integrated circuits such as bipolar integrated technology, NMOS technology and CMOS technology. In this Thesis, we have used CMOS technology. The main reason in using CMOS technology is due to its scalable high noise immunity and low power consumption [1]. Basically, CMOS technology uses both NMOS and PMOS, which means only either one of both types of transistors will be ON at a time during the operation. Thus, CMOS, IC consumes less power as power is used only when the NMOS and PMOS transistors are switching between on and off states [2] thus CMOS has better performance. Furthermore, the CMOS circuits are much cheaper if compared to other

technologies [3]. The concept of designing an IC for Bangla Alphabet character we got from the paper IC layout Design Of Decoder Using Electric VLSI Design System [4]. In present days Bangla Alphabetic Characters are represented using dot-matrics system [5, 6] where a large number of dots are to be manipulated. On the other hand for English Alphanumeric LED displays are available in three common formats [7]. For displaying only numbers and hexadecimal letters, simple 7-segment displays such as that shown in [7] are used. To display numbers and the entire alphabetic, 18-segments displays such as that shown in [7] or 5×7 dot-matrix displays such as that shown in [7] can be used. 11-segment display for Bangla and English numerals [8, 9], 12-segment for Bangla, English, and Arabic numerals, 9-segment for only English and Arabic digits [8], 9-segment [10] and 10-segment [11,12,13] for Bangla digits and 16 segments for multilingual [14] are already proposed. Since, Bangla Alphabetic characters are represented using dot metrics as a result the cost of the display unit increases due to storage space, a large number of dots, power loss, and design complexity. But recently very few researchers address the point to represent Bangla Alphabetic characters using segmented display unit [15,16,17,18]. Still there is no standard segmented display unit for Bangla Alphabetic characters. Moreover, to present the proposed 26-segmented display system is the most perfect and effective among all other display models [15,16,17,18] in terms of display quality, power loss, and design complexity. In this thesis we have used 26 segment displays because it's better than the other [19].

2.4 Problem discussion

There are a few technologies for constructing logic gate or integrated circuits such as bipolar integrated technology, NMOS technology, PMOS technology and CMOS technology and these different technologies can produce different IC. In this thesis, CMOS technology is used one of the reason CMOS is chosen over NMOS and bipolar technology is because CMOS circuit dissipates less power and PMOS show slow performance than CMOS. CMOS dissipates power only during switching and hence it has almost no static power dissipation. This factor has allowed the integration of more CMOS gates on an IC than in NMOS or bipolar technology, thus

CMOS has better performance. Furthermore, the of CMOS circuits is much cheaper if compared to other technologies. Many segment display model are available for bangle character display. At 17-Segment display unit for Bangla vowels. Shows the 17-segment display unit and shows its character sets. From its character sets it is observed that vowel □ is not clear enough. The quality of appearance is not good enough for all characters except □, □, □, and □ characters. Drawbacks of 17-segment for Bangla vowels are that the characters are not clear enough and the quality of characters is not good enough.

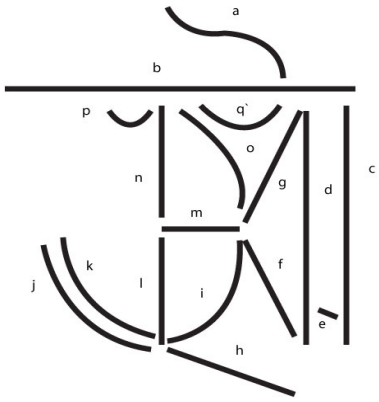
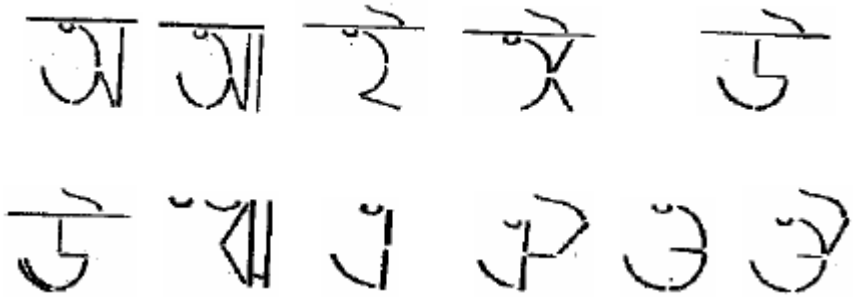


Fig.2.16: 17- Segment display



At 14-Segment display model only for vowels. shows the 14-segment display unit and shows its character sets. It covers only 11 Bangla vowels. The model is mainly based on straight lines. But the traditional Bangla vowel alphabets are not based only on straight lines. Many of them are based rather curved lines to a great extend. So, 14-segment display system for Bangla vowels

cannot be accepted a standard in the display system because, here, the proposed vowels are asymmetrical, and dissimilar and are, rather, not familiar to the users. The proposed alphabets are, also not identical to corresponding Bangla ones. This 14-segment model is not full, rather partial, as it is lacking in Bangla consonants and digits.

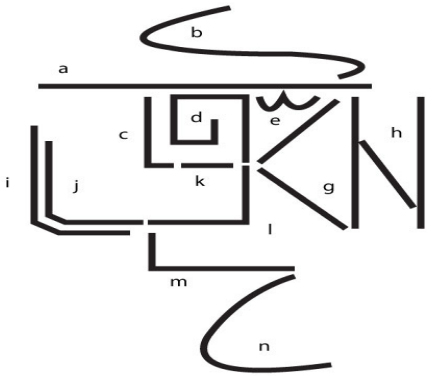
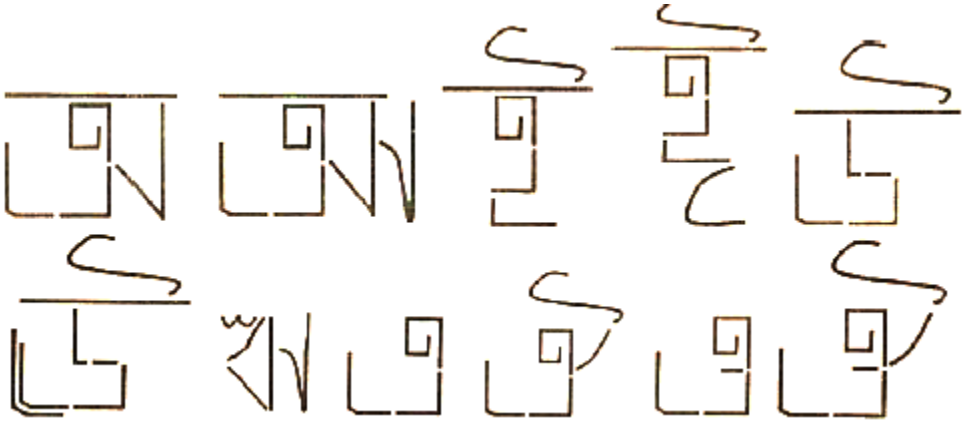


Fig.2.17: 14-Segment display

Fig.2.17: 14- Segment display



At 31-segment display unit and shows its character sets. The proposers claim that this display system has been proposed for Bangla characters, both digits and alphabets. But, here, we find 28 consonants and 6 digits only. Hence, it lacks 11 consonants and 4 digits. So, it does not cover all the Bangla alphabets and digits.

Many of the proposed characters are dissimilar to the original Bangla characters, such as □, □, □, □, □, and □ These are not also familiar to the users.

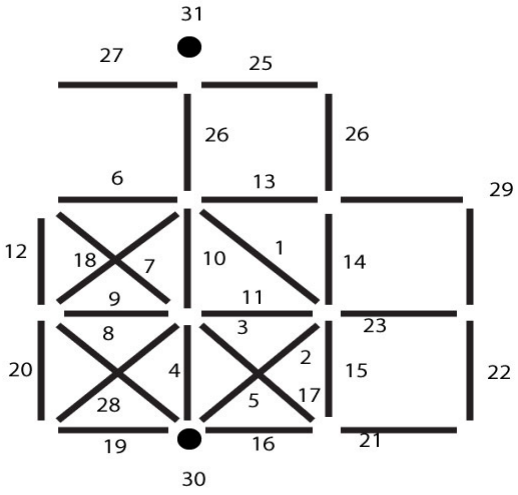
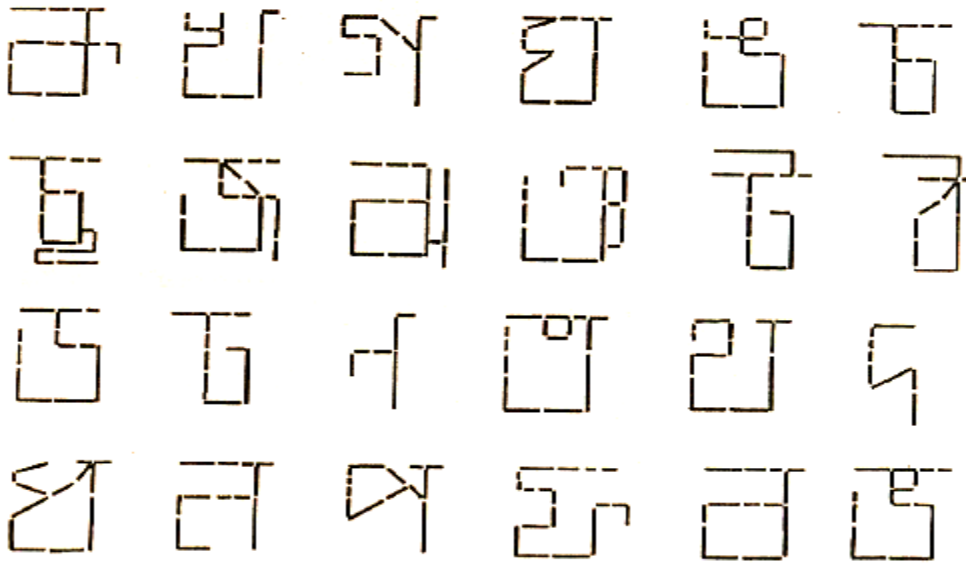


Fig.2.18: 31-Segment display

At 44-segment display model for consonants. shows the 44-segment display unit and shows its character sets. This model is proposed only for consonants. Some of the characters of this model are better than those of 31-segment display model. But some other characters are based on straight lines and, hence, are dissimilar to the original Bangla consonants such as □, □, □, □, □, □, □, □, □, □, and □



They have many limitation.Those limitations overcome by 26-segment display model [19].

2.5 Proposal

So, we have proposed CMOS technology for bangle alphabet IC design. Because it show better performance than other technology. And we have also proposed 26-segment display model. But for the joint word we have proposed the dot matrix display system.

2.6 Summary

Here we have studied about different types of gates and and different types of display and segment. We have studied about their operation, principle advantage and disadvantage. Later we have compared about different types of segment. We have analyzed their problems and advantages. Later we have chosen our favorite method.

CHAPTER 3 : METHODOLOGY

3.1 Introduction

Every thesis is a long term process. So we have sectionalized the entire process into 4 steps. First we have analyzed the entire following step theoretically and later we have compared our simulated data that means practical data with theoretical value. From this comparison we have followed this step to achieve our desired goal. Figure 3.1 shows the flow chart of the proposed IC design.

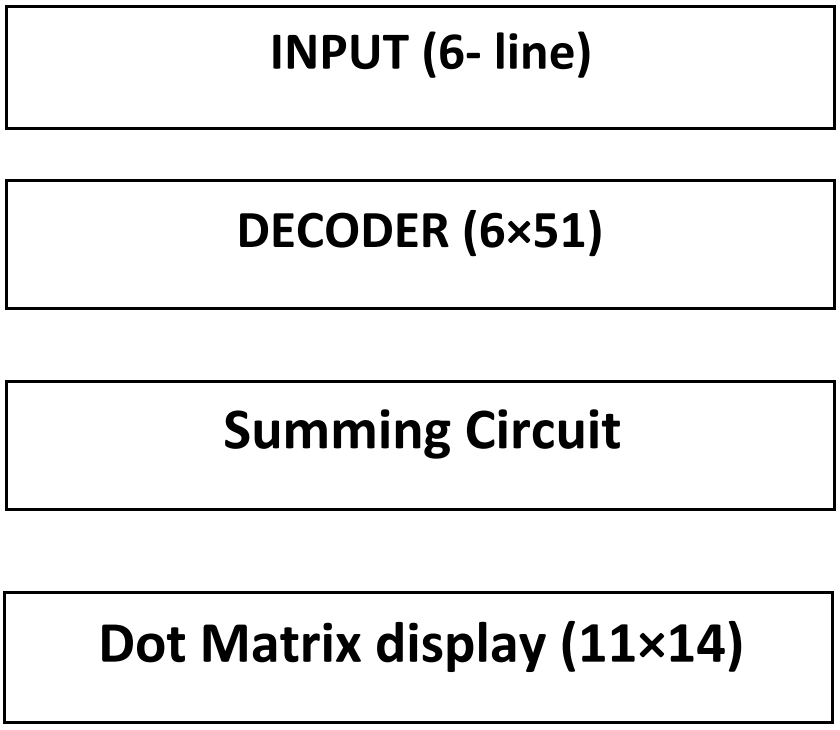


Fig.3.1: Flow chart of IC design.

3.2 Input

According to Bangla pedia there are 51 characters in Bangla. For this we have need 51 output signal. To get 51 signals it is required to have 6 signals as input line. By using this 6 input we can specify our desired output signal according to binary value. The magnitude of this DC voltage is always 5v.Since the construction of circuit is complex so any voltage less than 5v may be insufficient for the display to operate. Cause there is internal loss. Figure 3.2 shows the 6 input lines.

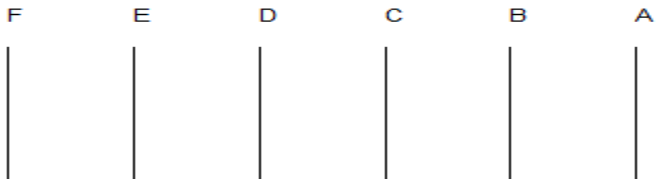


Fig.3.2: Input lines (6)

3.3 Decoder

A binary code of n bits is capable of representing up to 2^n distinct elements of the coded information .a decoder is a combination circuit that converts binary information from n input lines to a maximum of 2^n unique output line. Here we have used (6×51) decoder. That means the decoder collects the binary information from the 6 input lines and converts it into 51 output lines. Figure 3.3 shows the decoder circuit.

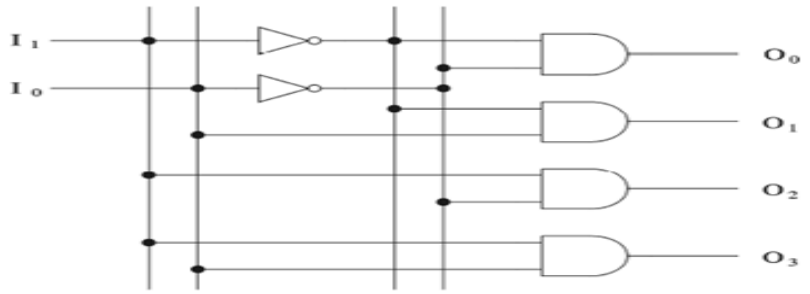


Fig.3.3: Decoder circuit (2×4)

3.4 Summing circuit

The main objective of summing circuit is to collect the decoder information for one segment of display. In description we can say it collects the output signal of decoder to determine which segment of the display will be on and which will be off .summing circuit can easily made by OR logic gate. Figure 3.4 shows the schematic diagram of summing circuit.

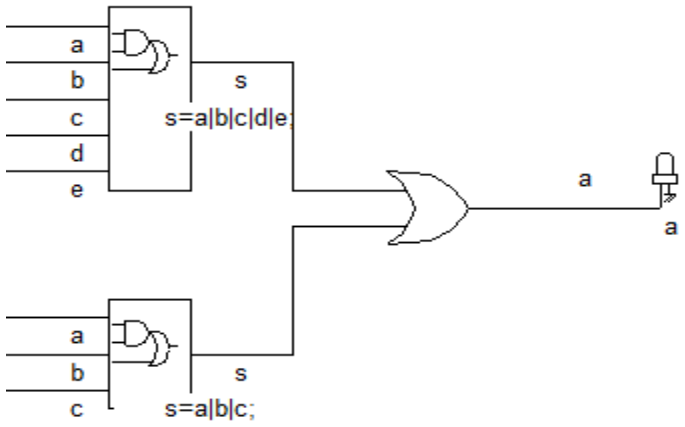


Fig.3.4: Schematic diagram of a summing circuit

3.5 26-Segments Display

Here, we use 26-segment Display as a display unit for bangle characters. There are many previous proposed segment display models for bangle character. But they have many limitations.17-segment display unit form Bangla vowels. From its character sets it is observed that vowel □ is not clear enough. The quality of appearance is not good enough for all characters except □ □, □ and □ characters. Drawbacks of 17-segment for Bangla vowels are that the characters are not clear enough and the quality of characters is not good enough. 14-Segment display model only for vowels. It covers only 11 Bangla vowels. The model is mainly based on straight lines. But the traditional Bangla vowel alphabets are not based only on straight lines. Many of them are based rather curved lines to a great extend. So, 14-segment display system for Bangla vowels cannot be accepted a standard in the display system because, here, the proposed vowels are asymmetrical, and dissimilar and are, rather, not familiar to the users. The proposed alphabets are, also, not identical to corresponding Bangla ones. This 14-segment model is not full, rather partial, as it is lacking in Bangla consonants and digits. 31-segment display model for Bangla characters. The proposers claim that this display system has been proposed for Bangla characters, both digits and alphabets. But, here, we find 28 consonants and 6 digits only. Hence, it lacks 11 consonants and 4 digits. So, it does not cover all the Bangla alphabets and digits. Many of the proposed characters are dissimilar to the original Bangla characters, such as □, □ □, □, □, and □ These are not also familiar to the users. 44-segment display proposed only for consonants. Some of the characters of this model are model for consonants. This model is better than those of 31-segment display model. But some other characters are based on straight. But 26-segment display model overcome such type of limitation.

So we use 26-segment display unit for bangle characters. It is not very much convenient for creating joint word. Table 3.1 shows the truth table for Bangla alphabet character display.

Table 3.1: Truth table for Bangla Alphabet character Display

SL		F	E	D	C	B	A	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z
0	অ	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0
1	আ	0	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0
2	ই	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0
3	ঈ	0	0	0	0	1	1	1	0	0	0	0	1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0
4	উ	0	0	0	1	0	0	1	0	1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
5	ঊ	0	0	0	1	0	1	1	1	1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
6	ঋ	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1	1	1	0	0	1	0	0
7	এ	0	0	0	1	1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0
8	ঐ	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	1	1	1	1	0	0	0	0	1	0
9	ও	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	ঔ	0	0	1	0	1	0	0	1	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0
11	ক	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0
12	খ	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	1	1	1	0	0	1	0	0	0
13	গ	0	0	1	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0
14	ঘ	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0

3.6 Matrix Display

Since, we are unable to represent the joint word through the IC. So we have tried it with Dot Matrix display. And at last we can do it with the Dot matrix display. One of the advantages of dot matrix display is the complex and diverse character can be design by it. Here we have used (11×14) dot matrix display. Figure 3.5 shows the interconnection of dot-matrix Display. Figure 3.5 shows the interconnection of dot-matrix display.

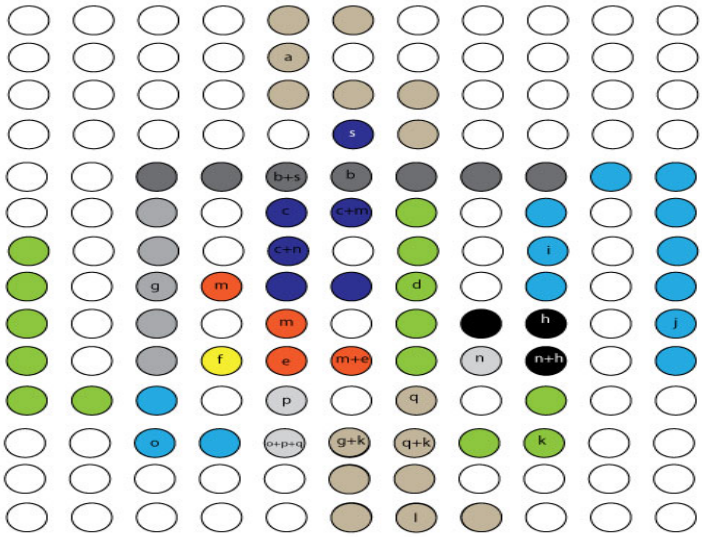


Fig.3.5: Interconnection of dot-matrix Display (11×14).

We have analyzed about the dot matrix display and bangle alphabet character. The following table shows truth for bangle alphabet character for dot matrix display.

Table 3.2: Truth table for dot matrix display.

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s
□	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
□	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
□	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0
□	1	1	1	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0
□	1	1	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
□	1	1	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0
□	0	1	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1
□	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0
□	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
□	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0
□	1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0

Later we have tried to reduce the matrix number and finally we have proposed the following table which shows the interconnected dot matrix.

Table 3.3: Interconnected dot matrix

Name of Interconnection	Matrix number (position)
a	**M_14, M_15, M-24, M_34, M_35, M_36, M_46, M_56.**
b	**M_52, M_53, M_54, M_55, M_56, M_57, M_58**
c	**M_64, M_65,M_74,M_84, M_85**
d	**M_66, M_76, M_86, M-96,M_106**
e	**M_104, M_105**
f	**M_103**
g	**M_62,M_72,M_82,M_92,M_102**
h	**M_97,M_98, M_108,**
i	**M_68,M_78,M_88**
j	**M_59,M_510,M_610,M_710, M_810, M_910, M_1010**
k	**M_118,M_128.M_125,M_126,M_127,**

l	**M_135,M_145, M_147, M_146**
m	**M_75,M_84,M_95**
n	**M_107, M_108**
o	**M_112,M_122, M_123, M_124,**
p	**M_114,M_124,**
q	**M_124, M_125, M_126,M_116,**
r	**M_70,M_80,M_90, M_100, M_110, M_111**
s	**M_64,M_74,**

3.7 Summary

In the design process of this IC we have followed the above methodology step by step. In each step we have tried to make a comparison between theoretical and practical value. From this comparison we have tried to find out the deviation.

CHAPTER 4: Result and Discussion

4.1 Introduction

In this section we have analyzed our designed IC through different calculation. Here we have worked to find out the Boolean function. Time diagram, FFT (Fast Fourier Transform) of our designed IC .We has calculated the theoretical and practical Value. And try to find out the deviation between theoretical and practical value. We have calculated all the Boolean Function necessary for each segment.

4.2 Boolean function

Boolean Function for Bangla Alphabetic Characters

From the Truth Table 1.2, we can write the following logic functions
For different 26-segments in sum-of-product form:

a = Σ (0,1,2,3,4,5,12,15,17,18,19,20,22,23,24,25,27,29,31,33,34,35,
36,37,38,39,41,42,43,44,45,46);
b = Σ (5,9,10,24,35,44);
c = Σ (0,1,4,5,7,8,16,19,21,27,48,50);
d = Σ (4,5,17,18,19,22,24,25,29,44,45);
e = Σ (17,18,22,25,29,45);
f = Σ (0,1,3,4,5,7,8,9,10,16,17,18,19,21,22,24,25,27,29,35,42,44,45,47,50);
g = Σ (16,40);
h = Σ (6,13,15,16,30,35,36,47);
i = Σ (0,1,2,3,6,7,8,9,10,11,13,16,21,26,27,28,30,35,40,43,47,48,49,50);
j = Σ (0,,1,2,3,9,10,11,14,19,27,28,32,33,37,41,42,43,46);
k = Σ (0,1,2,3,4,5,6,9,10,12,13,15,16,17,18,19,20,22,23,24,25,27,28,
29,30,33,34,35,36,37,38, 41,42,43,44,45,46,47,50);
l = Σ (4,5,9,10,17,18,19,24,44);
m = Σ (31,36,38,39,44,45,46,49);
n = Σ
(0,1,2,3,6,7,8,12,13,15,18,20,21,23,28,30,31,33,34,36,37,38,39,41,42,43,46);
o = Σ (19,41);
p = Σ (3,10,11,12,20,23,30,32,34,38,50);
q = Σ (7,8,14,21,26,32,40);
r = Σ (0,1,6,7,8,12,13,15,20,21,23,28,29,30,31,33,34,36,37,38,39,41,42,46);
s = Σ (0,1,6,7,8,12,13,14,15,20,21,23,26,28,30,31,32,33,34,36,37,38,40,41,42,46);
t = Σ (0,1,6,8,10,11,12,13,14,15,20,26,28,30,31,32,34,36,37,38,40,41,42,46);
u = Σ (6,20,39);

v = Σ (21);
w = Σ (12,21,33);
x = Σ (1,6,20,39);
y = Σ (2,3,4,5,8,10,11,22,23);
z = Σ (40);

4.3 Schematic diagram

We have decorated our required AND gate, OR gate, decoder and summing circuit with nMOS and pMOS. Later we have interconnected that element. Finally we get this kind of schematic diagram.

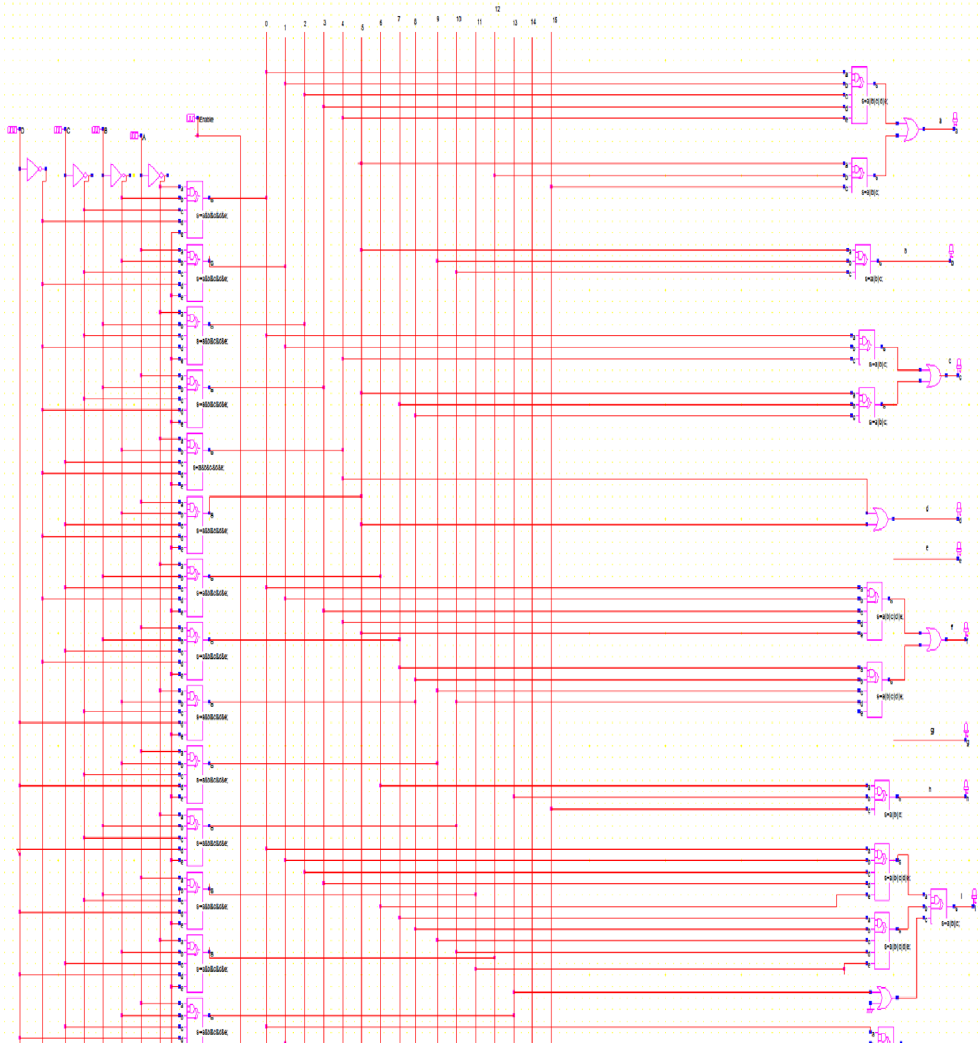


Fig.4.1: Schematic diagram of IC

The following shows a clear view of our designed IC.

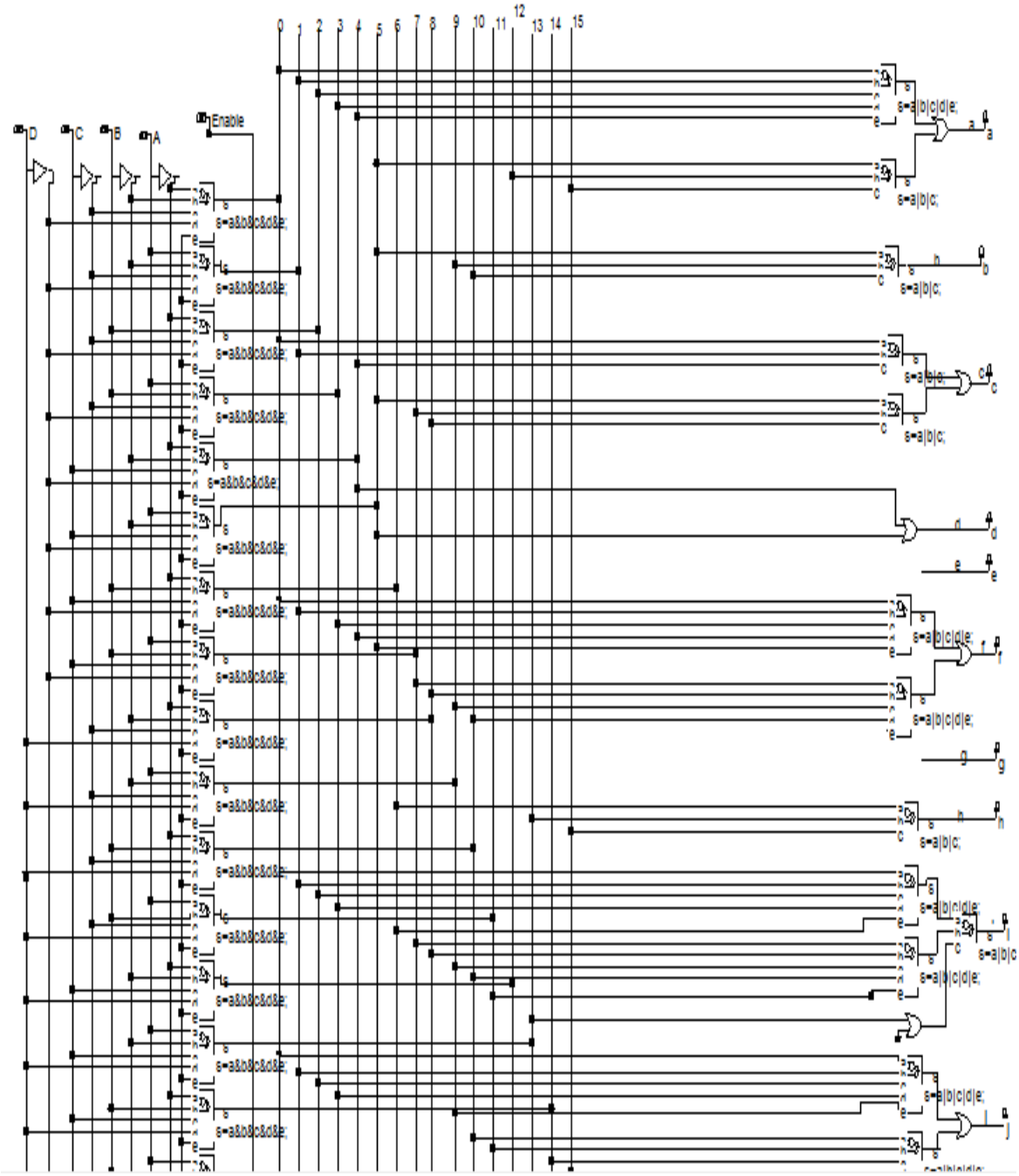


Fig.4.2: Clear view of a section of IC

We have followed the basic parameter for designing our IC .So that we can avoid the cross connection and can get our desired output. The following table shows those parameter followed by us.

Table 4.1: Design rule for IC layout

Well	Measurement
Minimum well size	12 ʎ
Between well	6ʎ
Between N-Well and P-well	0ʎ
Minimum well area	12ʎ×12 ʎ
Polysilicon1	2 ʎ
Polysilicon 1 width	2ʎ
Between polysilicon 1s	3ʎ
Between polysilicon 1 and metal	N/A
Minimum polysilicon area	2ʎ×2 ʎ
Metal 2,3,4,5	2ʎ
Metal width	3ʎ
Between Metals	3ʎ
Between Metal and other metal	N/A
Minimum metal area	3ʎ×3 ʎ

4.4 Layout

After designing our desired IC we have found this layout. From this viewer can identified how metal, polysilicon, substrate interconnected with each other.

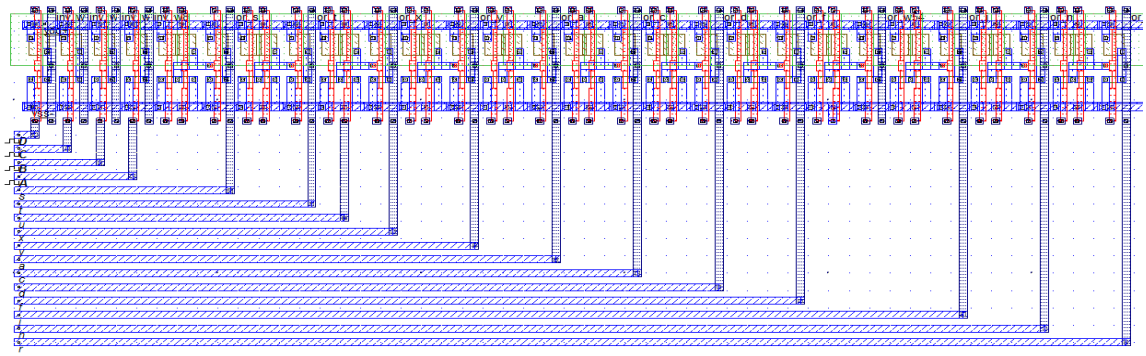


Fig.4.3: layout of the designed IC

4.5 Practical Performance

Later we have tasted our IC. We have checked out our connection through the performance test. We have done it for several times. Here is an example given below in Fig 4.4. We have tested our IC several times for different characters through time diagram. Fig 4.5,4.6,4.7,4.8,4.9,4.10 show the time diagram respectively for □,□ ,□,□,□,□.

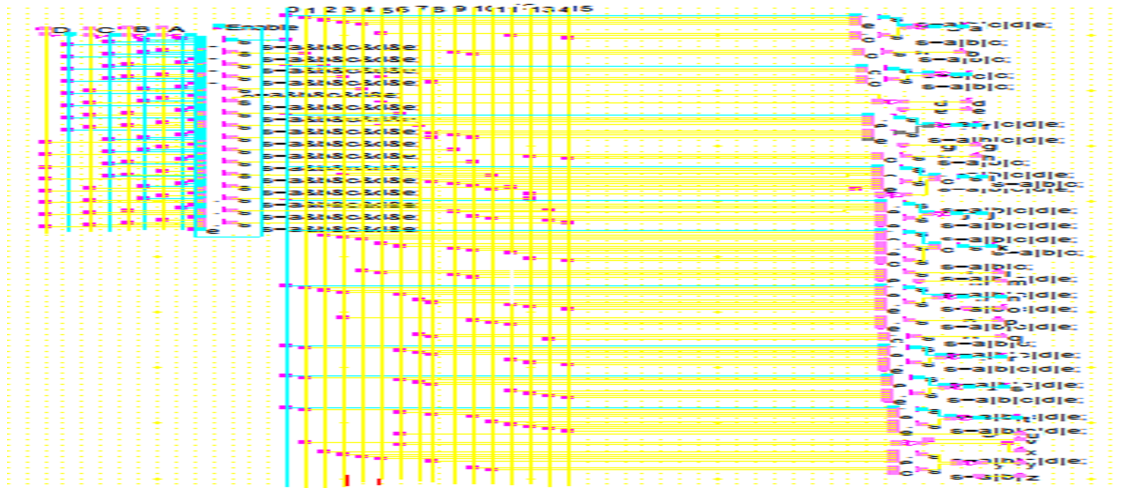


Fig.4.4: Performance Test for □

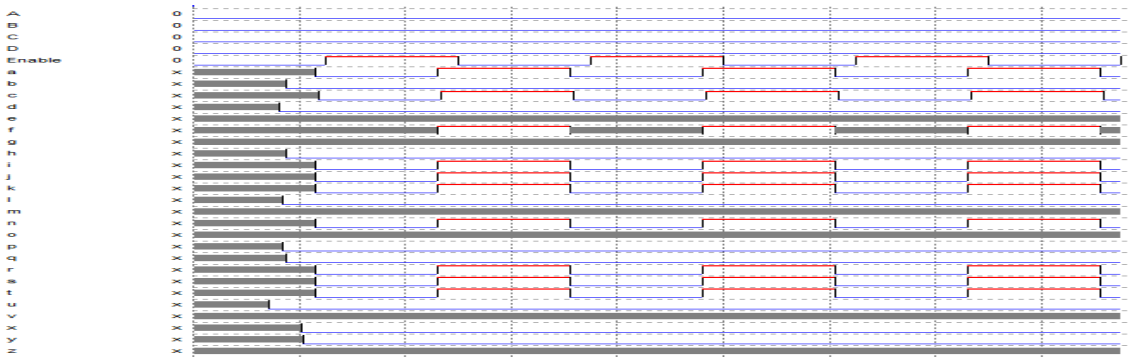


Fig.4.5: Time diagram for □

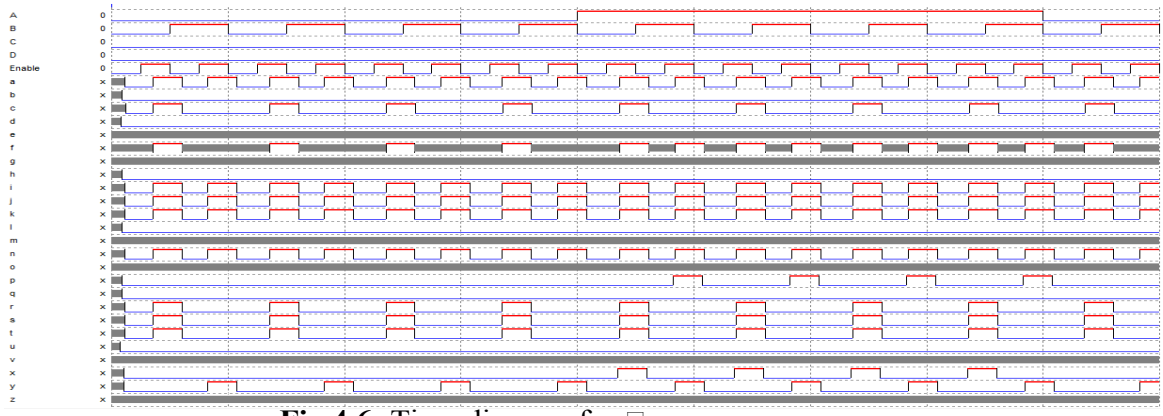


Fig.4.6: Time diagram for □

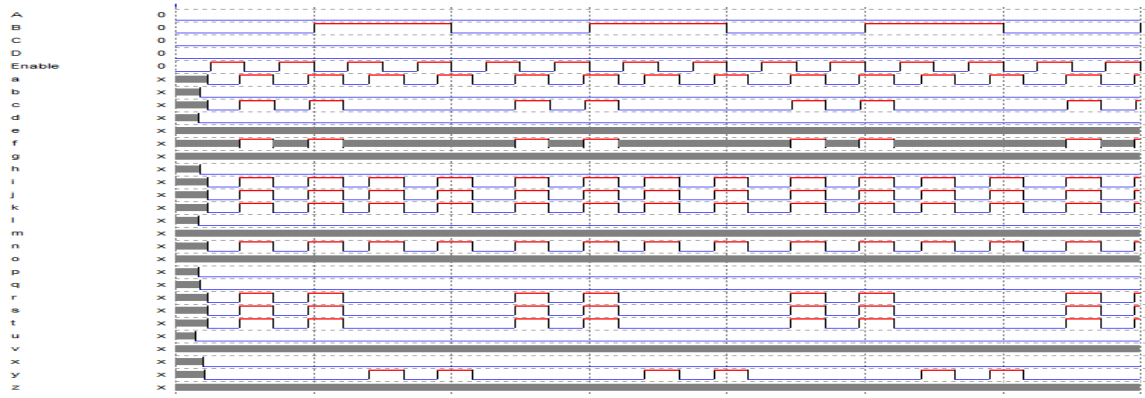


Fig.4.7: Time diagram for □

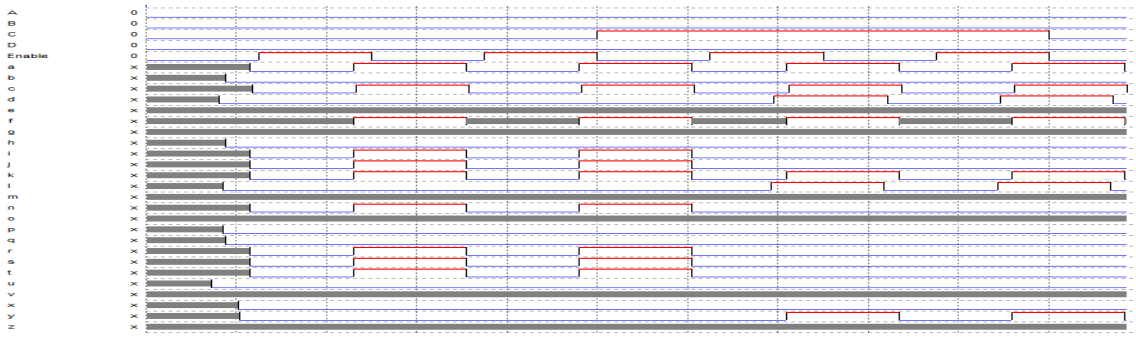


Fig.4.8: Time diagram for □

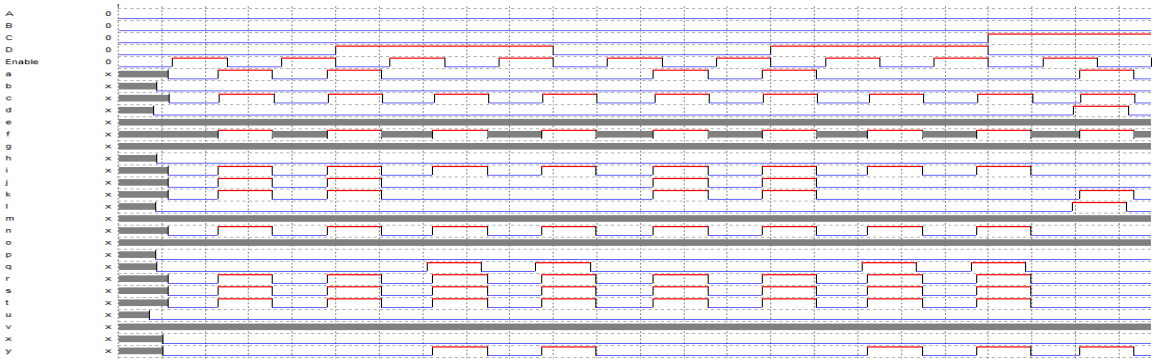


Fig.4.9: Time diagram for □

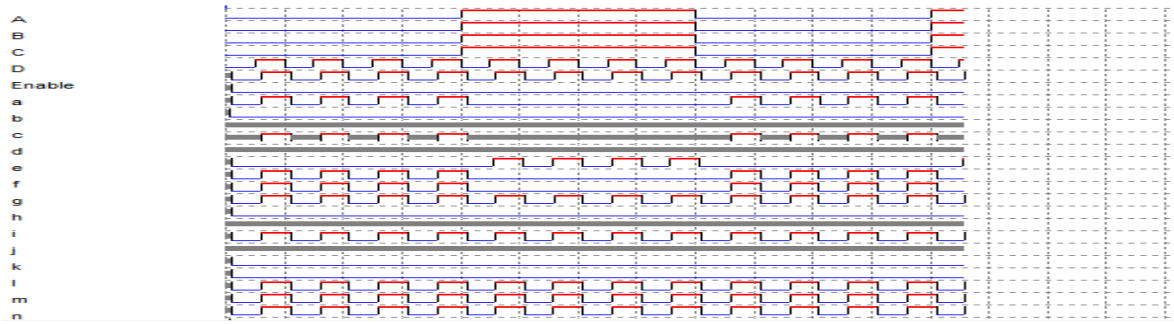


Fig.4.10: Time diagram for □

After testing the performance of our designed IC we have calculated the no of gate required for our designed IC. The following tables show that calculation.

Table 4.2: Calculation of MOSFET for AND gate

Input	AND gate	Total NO of MOSFET	NMOS	PMOS
5	51	612	306	306

Input	NOT gate	Total no of MOSFET	NMOS	PMOS
1	6	12	6	6

Table 4.3: Calculation of MOSFET for NOT gate

Table 4.4: Total Calculation of MOSFET for The designed IC

Gate type	NMOS	PMOS	Total no of MOS
OR	336	336	672
AND	306	306	612

NOT	**6**	**6**	**12**
Total	**648**	**648**	**1296**

Power consumption through IC

Voltage=1.2v

Current=0.035mA

Power=0.042mW

4.6 Designed IC

After performance testing and calculation of necessary gate we have found this type of structure of our designed IC. Figure 4.11 shows the external view of our designed IC.

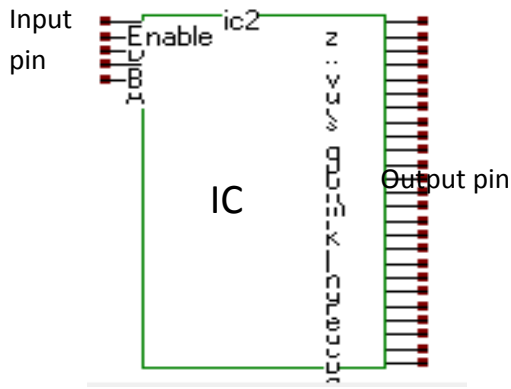


Fig.4.11: External View of IC (4 input –output 15)

4.7 Bangla Alphabet Character design in Dot Matrix display

Since 26 segment display is not applicable for joint word we have choose the dot matrix display. Then by following the previous method we have designed an IC for dot matrix display. We have interconnected those entire required element. Then we have found these

types of schematic diagram. Figure 4.12 shows the schematic diagram of our designed IC for dot matrix display. Later we have again tested the performance of our newly built IC. The following figure shows a view of performance testing for different Bangla word through time diagram.

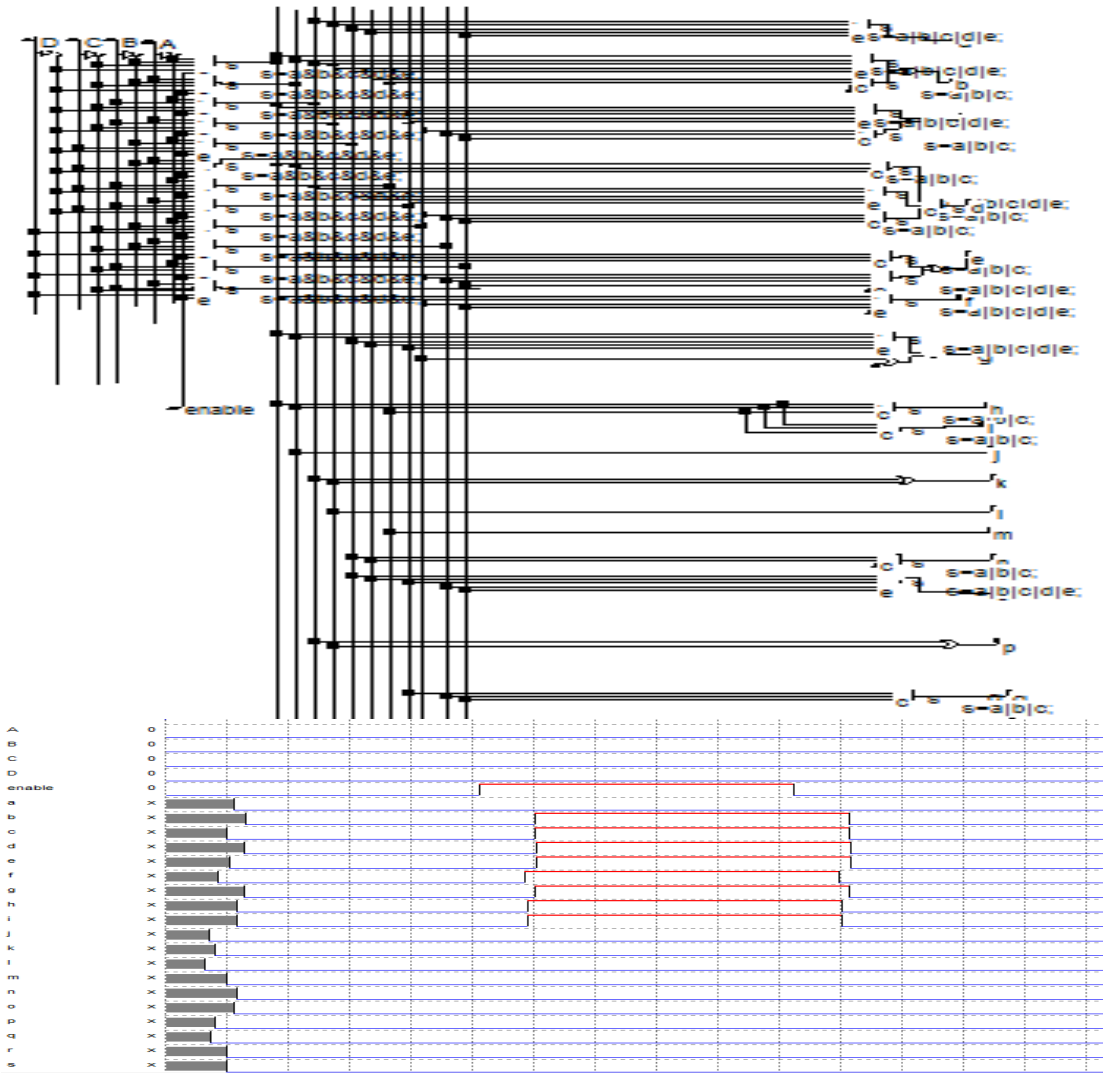


Fig.4.13: Time diagram for □

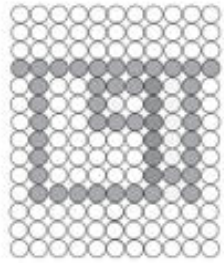
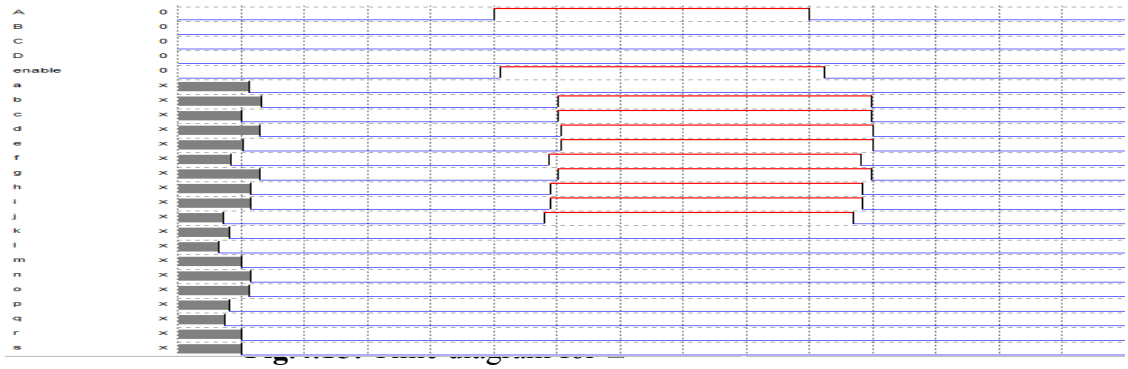
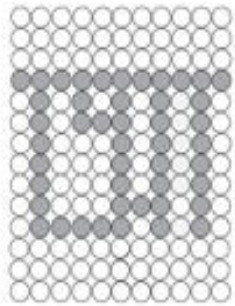
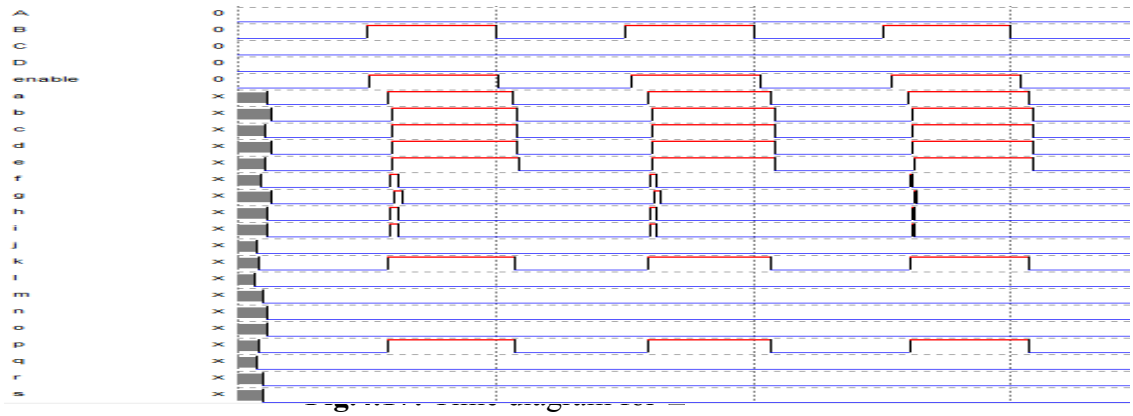


Fig.4.14: Dot matrix view for □







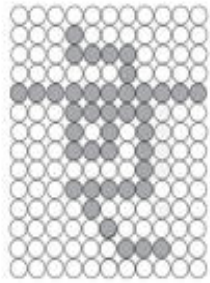


Fig.4.18: Dot matrix view for □

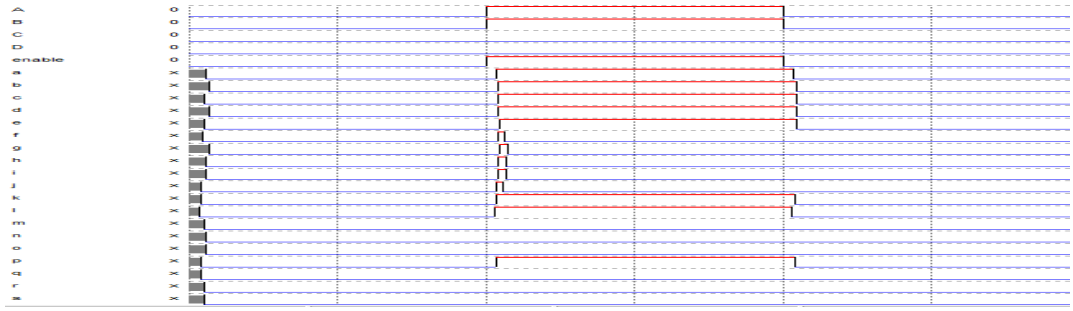


Fig.4.19: Time diagram for □

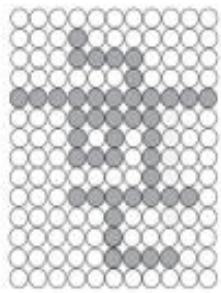


Fig.4.20: Dot matrix view for □

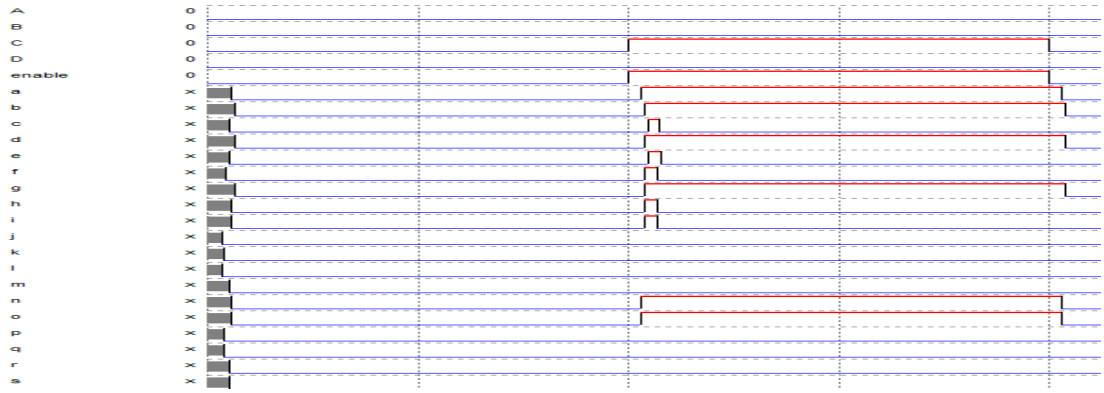


Fig.4.21: Time diagram for □

Fig.4.22: Dot matrix view for □

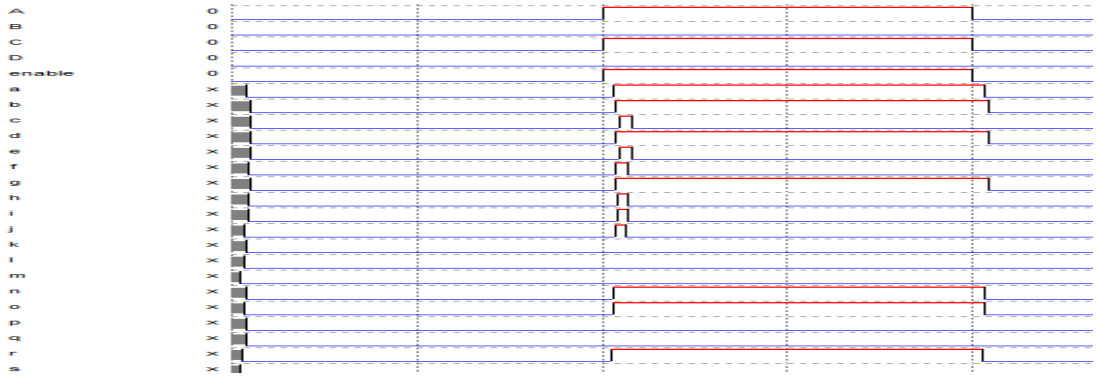


Fig.4.23: Time diagram for □

Fig.4.24: Dot matrix view for □

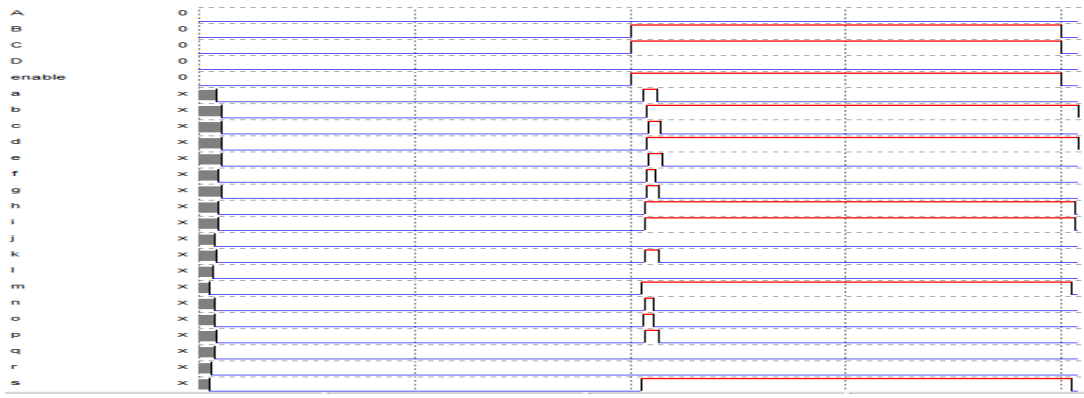


Fig.4.25: Time diagram for □

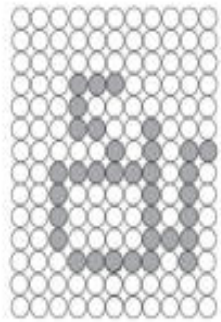


Fig.4.26: Dot matrix view for □

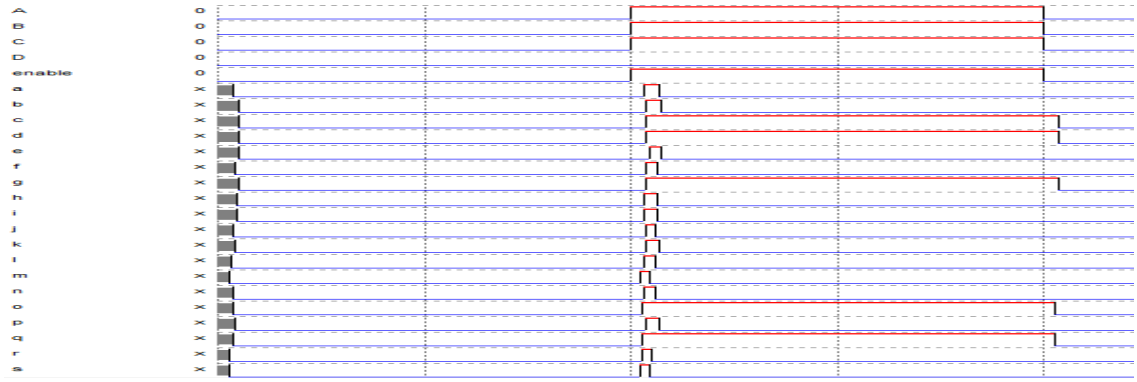


Fig.4.27: Time diagram for □

Fig.4.28: Dot matrix view for □

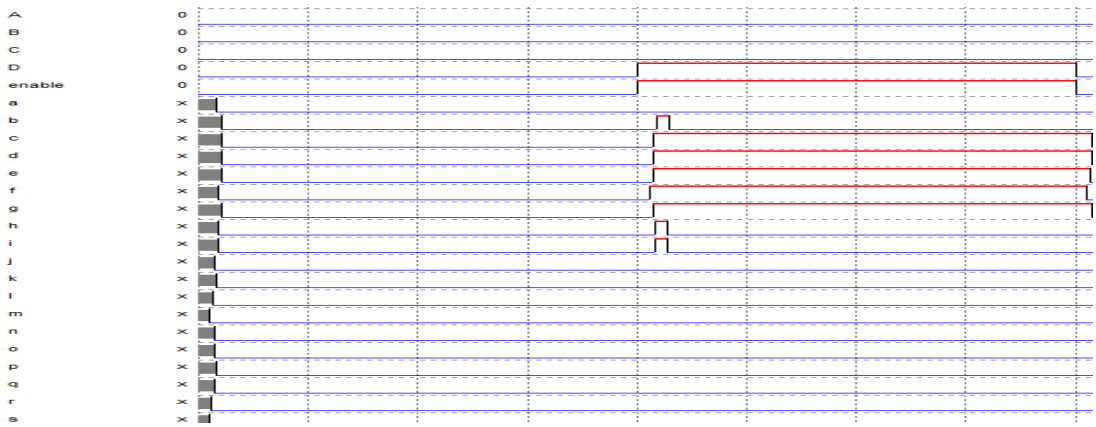


Fig.4.29: Time diagram for □

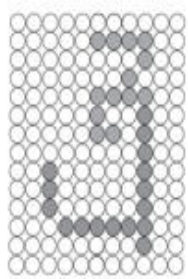


Fig.4.30: Dot matrix view for □

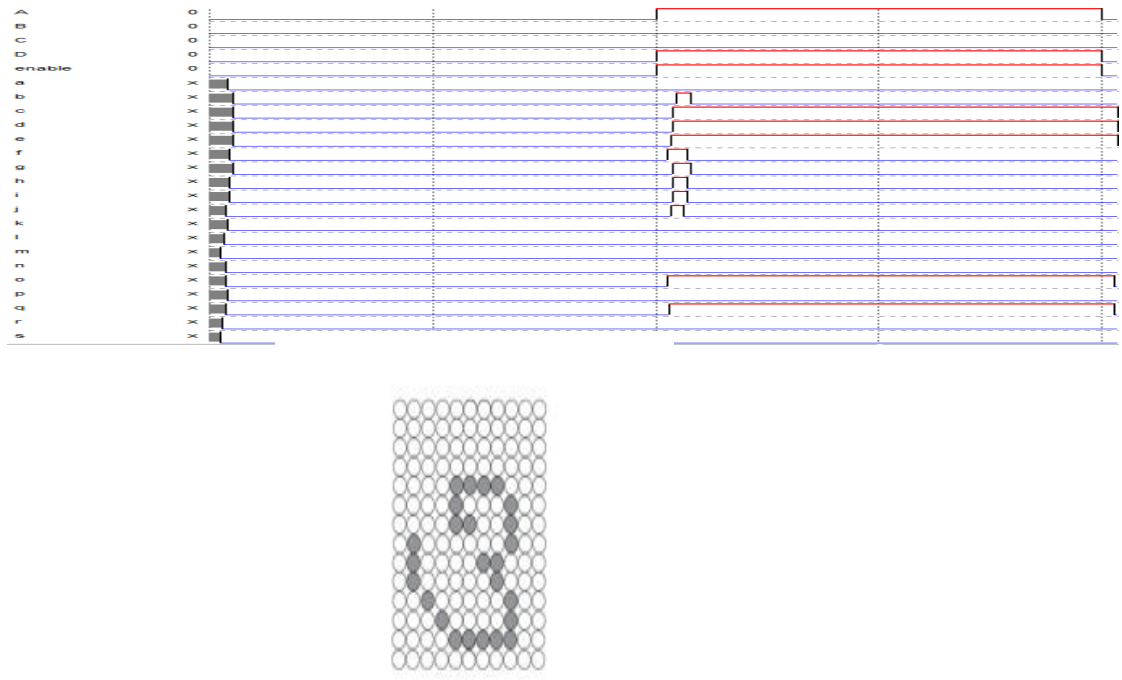


Fig.4.32: Dot matrix view for □

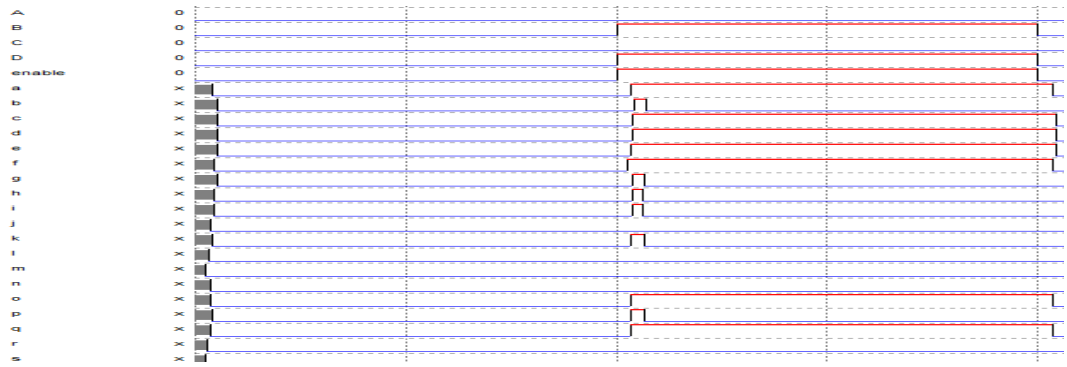


Fig.4.33: Time diagram for □

Fig.4.34: Dot matrix view for □

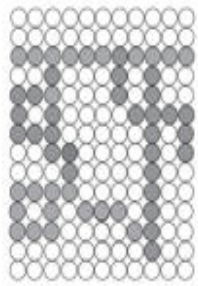


Fig.4.35: Dot matrix view for □□

4.8 Designed IC

After performance testing and calculation of necessary gate we have found this type of structure of our designed IC. Figure 4.36 shows the external view of our designed IC. And this is our final designed IC.

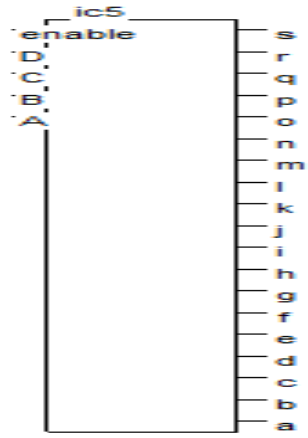


Fig.4.36: External View of Designed IC for Dot Matrix display

Power consumption through IC (dot matrix)

Voltage=1.2V

Im=3.00mA

Current (avg) =0.006mA

Power=0.007mW

Total Power=0.448mV

4.9 Discussion

In the ongoing process at first we have analyzed the segment of the display. Then we have identified the necessary input for each of the 51 BANGLA ALPHABET character. Then we have designed a decoder to customize the signal. But on the ongoing process we have faced some problem. Such we have noticed that we do not get our desired output in the display

immediately after enabling the enable pin. It starts after a few moments. Then we try to find the reason behind it. Then we have found some of the following reason. This circuit is a complex circuit. And most of the gate was designed with CMOS .We know that the switching action of MOS is largely depends on the length of channel. Due to this huge length the switching action may become slow. Another reason may be the interconnection. Since we have made the interconnection by metal contact so this also causes some metallic loss .This loss also included with the previous reason to slow the action of MOS. Here we have used Dot matrix display to design the diverse and complex character. By the dot matrix display we can give the character different types of shape.

CHAPTER 5: CONCLUSION

5.1: Introduction

In this thesis it has been show how to activate different segment to have a successful display of all the Bangla Alphabetic characters through our proposed IC. If we take the entire factor in consideration then we found that the proposed system is better in all respect. Since there were a little work had been made in this field, it's our little endeavor to make this possible through IC based Bangla Alphabet technology. To the best of our knowledge this attempt will help to improve the Bangla alphabet technology in near future.

5.2 Limitations

Though we have tried our best but we have found some limitation of this thesis.

- First of all the response of our designed IC is slow. That means it does not give output immediately after the input signal. But today's digital world always demands fast response from any newly designed technology.

- It also have some other limitation such as our designed IC cannot make the Bangla joint alphabet such a □□, □□, □□, □□, □□, □□, □□, □□, □□, □□, etc.

5.3 Suggestions

Since our designed circuit is little bit complex

- We can reduce the complexity of the circuit through k-map analysis.

- We can make it more compact.

- We can reduce the number of required segment it will give faster response.

5.4 Future plans

- Make it capable to make the joint Bangla Alphabet.

- Reduce the complexity

- Try to increase the number of character in same display.

5.5 Overall conclusion

In this chapter we have discussed about the limitation and difficulties of our designed IC. Later we have given some new to make it more compact and user friendly such as addition of bangle joint Alphabet, increasing the speed of response reducing complexity etc. We started this thesis to represent Bangla and enhancing the use of Bangla Alphabet character in modern technological world. On this road we have faced difficulties about selection of segment, design process of the gate, selection of MOSFET, design process of decoder etc. At last we have found that our designed IC is very much capable to contribute in print sector more efficiently than any of the previously designed method. In this design process we take the assistance from DSCH and Microwind software. But after designing our desired IC we have tested it frequently. Then we have found some limitation of our IC which we have discussed earlier. Later we have made some suggestion to overcome this limitation and how to make it more users friendly, compact simple and faster. We have also found some difference between

the wave shape of theoretical and simulated output. It happened due to the presence of noise in the basic gate.So it is very much recommended that to design the gates without noise.

REFERENCES

[1] S.H.Teen, L..L.Lim and J.H. Lim; IC Layout Design of Decoder Using Electric VLSI Design System, International Journal of Electronics and Electrical Engineering Vol. 3, No. 1, February, 2015.

[2] R.J. Baker, CMOS: Circuit Design, Layout, and Simulation, John Wiley & Sons, 2010, pp. 6-12.

[3] R.Behzad, "Design of analog CMOS integrated circuits,"McGraw-Hill Higher Education, New York, 2001.

[4] V. HALL; Microprocessor and Interfacing, McGraw-Hill Higher Education, New York, 2010. PP.4,54,164-165,227, 267.

[5] WILKINSON, BARRZ & HORROCKS, DAVID; Computer Peripherals, John Wiley & Sons, 2006. PP.6-7, 29-36.

[6] V. HALL; Microprocessor and Interfacing, McGraw-Hill Higher Education, New York, 2010. PP.4,54,164-165,227, 267.

[7] M.O.AZIM, M.A.CHOWDHURY, M.S.& ISLAM, M.N.;(2003); Different Segment displays for Bangla, English and Arabic digits, 6th ICCIT 2003, Jahangirnagar University, PP. 299-302, December 19-21.

[8] Designing 11-Segment Display for Bangla Digits, 5th ICCIT 2002, East West University, Dhaka, PP. 237, December 27-28.

[9] N. & KHAN, M.M.R., Designing 9-segment Display for Bangla Digits, Proceeding of the ICEECE 2003, Dhaka, Bangladesh, PP. 42-45, December 22-24.

[10] S.M., KHAN, M.S.I., RAHMAN, S.M.M., & ALI, M. (2003); Designing 10-segment Display for Bangla Digits, Proceeding of the ICEECE 2003, Dhaka, Bangladesh, PP. 161-164, December 22-24.

[12] ARIFIN, S.M.N., MEHEDY, L., & KAYKOBAD, M. (2003); Segmented Display for Bangla Numerals: Simplicity vs. Accuracy, 6th ICCIT 2003, Jahangirnagar University, PP. 199-125, December 19-21.

[13] HOSSAIN, G. & HABIB, A.H.M.A. (2003), Desiging Numeric Characters Twin Display By –7 Segments, 6th ICCIT 2003, Jahangirnagar University, PP. 317-320, December 19-21.

[14] TALUKDER, A.K.M.K.A. & ROY, K. (2003); Development of 16-segment Multilingual Display Driver, Proceeding of the ICEECE 2003, Dhaka, Bangladesh, PP. 27-31, December 22-24.

[15] ISLAM, A.K.M.N., MAHMUD, S.M.M., SHAHRIER, N., & SATTAR, M.A. (2003); Designing 17-segment Display for Bangla Vowels, 6th ICCIT 2003, Jahangirnagar University, PP. 283-286, December 19-21.

[16] MASUM, S.M. & AL-MAMUN, M.A. (2005); Designing 14-Segment Display for Bengali Vowels, Asian Journal of Information Technology, Grace Publications Network, Vol. 4 No. 2, PP. 178-184.

[17] MAHMUD, S., AREFIN, A.S., & KHAN, M.I. (2005); A New Approach for Displaying All Bengali Characters, Asian Journal of Information Technology, Grace Publications Network, Vol. 4 No. 2, PP.194-197.

[18] MASUM, S.M., HAQUE, S.M., DASH, S.C., & KABIR, K.F. (2005); Segmented Display System for Bengali Consonants, Asian Journal of Information Technology, Grace Publications Network, Vol. 4 No. 2, PP. 291-300, 2005.

[19] M. O. Rahman and M. A. Khan; Display Unit for Bangla Characters, ISSN 1813-7733 Vol. – 4, December 2007 Published in April 2008 (p 71-86).

[20]