International Islamic University Chittagong (IIUC)

Department of Computer and Communication Engineering

Semester End Examination

Program: **B.Sc. (Engg.)**
Course Code: **CCE -3509**
Total Marks: **50**

Semester: **Autumn 2024**
Course Title: **Computer Architecture**
Time: **2 Hours 30 Minutes**
Date: 06/01/2025

(i) Answer all the questions. The figures in the right-hand margin indicate full marks.
(ii) Course Learning Outcomes (CLOs) and Bloom's Levels are mentioned in additional Columns.

Course Learning Outcomes (CLOs) of the Questions

CLO1	Understand the Overview, Computer System, Arithmetic and logic, Central processing unit and parallel organization.
CLO2	Understand the Computer and Processor Design, Hazards; Exceptions; external and internal memory Pipeline and multiple processor systems.
CLO3	Develop and design an instruction set architecture and subsystems of central processing unit.

Bloom's Levels of the Questions

Letter Symbols	**R**	**U**	**Ap**	**An**	**E**	**C**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

PART-A

[Answer two questions from the following]

Q1.	a)	Describe the concept of pipelining in computer architecture and discuss its impact on improving system performance.	**CLO2**	**U**	4
	b)	Explain the working of the asynchronous pipeline model, focusing on how data flows through its stages without relying on a global clock signal.	**CLO2**	**An**	6
Q2.	a)	In which addressing mode the operand is available in the instruction itself – explain with an example.	**CLO1**	**U**	4

	b)	Consider the following assembly code snippet:
		`MOV R1, #10;`
		`MOV R2, [500];`
		`ADD R1, [R2];`
		i. Identify the addressing mode used in each instruction.
		ii. Analyze how the choice of addressing mode affects memory access and CPU cycles required to execute this code.
			CLO1	**An**	6

OR

Q2.	a)	What is meant by Addressing modes? What role do Addressing modes play in instruction execution?	**CLO1**	U	4
	b)	Analyze the efficiency of immediate addressing mode in reducing memory access compared to indirect addressing. Explain with an example.	**CLO1**	An	6

PART-B

[Answer three questions from the following]

Q3.	a)	Enumerate the characteristics of RISC architectures.	CLO3	U	4
	b)	RISC processors are expected to achieve higher throughput - Justify the statement with proper RISC architecture.	CLO3	E	6
Q4.	a)	Between a Write Through and Write Back cache, which one will generate less memory traffic - Explain your answer.	CLO1	An	4
	b)	Consider a multiprocessor system where multiple caches are involved in maintaining coherence. The system uses the Snoopy Bus Protocol. i. Explain how the Snoopy Bus protocol works to maintain cache coherence among the caches. ii. Compare this with a Directory-Based Protocol, discussing how it addresses the same problem differently.	CLO1	An	6
Q5.	a)	Write a short note on Register Renaming.	CLO2	U	4
	b)	Given the instruction sequence: 1. ADD R1, R2, R3; 2. SUB R4, R1, R5; 3. MUL R6, R4, R7; i. Identify and explain any Read After Write (RAW) hazards in the given sequence. ii. Calculate the number of stalls required to resolve the hazard without forwarding.	CLO2	An	6

OR

Q5.	a)	What do you understand by hazard in a pipelined processor? What are the different types of hazards?	CLO2	U	4
	b)	With a neat block schematic, explain a 3-stages Non-Linear Pipeline for two output functions and give processing sequence and reservation table for both functions.	CLO2	An	6

**** Good Luck ****