International Islamic University Chittagong
Department of Computer &Communication Engineering

Semester: **Autumn-2021**
Course Code: **CCE-2411**
Time: **2.5 Hours**

Program: **B.Sc. Engg. (CCE)**
Course Title: **Digital Logic Design**
Full Marks: **50**

Part A

[Answer any two of the following questions; Figures in the right margin indicate full marks.]

1(a).	Explain Why NAND Gate is said to be Universal Gate.	**CLO1**	**02**
1(b).	Differentiate between Half Adder and Full Adder Circuit. Formulate the Logical expressions output Sum and Carry for a full Adder circuit.	**CLO2**	**08**
2(a).	Design a combinational logic circuit that can converts 2,4,2,1 to 8, 4, -2-1 code.	**CLO2**	**06**
2(b).	Using the block diagram method, implement the following function using only NAND gates. $$F=A(B+CD)+B\overline{D}$$	**CLO2**	**04**
3(a).	Explain the necessity of parity generator and checker logic circuit during the transmission of binary information.	**CLO2**	**02**
3(b).	Design a combinational circuit to generate and check for even parity of three bits message of 4, 2, 1 weighted binary code.	**CLO2**	**08**

Part B

[Answer any two of the following questions; Figures in the right margin indicate full marks.]

4(a).	Explain the procedure to reduce the carry propagation delay in 4-bit binary parallel adder.	**CLO2**	**04**
4(b).	Implement the following function with a multiplexer, $$Y(A, B, C, D) = \sum(0,2,3,6,8,11,15)$$ Consider the variable B in the multiplexer input and A, C, D to the selection lines of an 8×1 *MUX.*	**CLO2**	**06**
5(a).	Design a **4X16** Decoder by using only **2X4** decoders.	**CLO2**	**04**
5(b).	Design a combinational circuit using a ROM. The circuit accepts a 3-bit binary number and generates an output binary number equal to the cube of the input number.	**CLO2**	**06**
6(a)	Differentiate between Read Only Memory (ROM) and Programmable Logic Array (PLA).	**CLO1**	**03**
6(b)	A combinational circuit is defined by the functions: $$F_1(A,B,C)=\sum(3,5,6,7),\ F_2(A,B,C)=\sum(0,2,4,7)$$ Implement the circuit with PLA.	**CLO2**	**07**
7(a)	Illustrate the limitations of clocked S-R flip-flops and Describe the operation of a flip-flop in which these limitations can be overcome.	**CLO1**	**05**
7(b)	Design a counter that has a repeated sequence of four states as shown in the state diagram.	**CLO2**	**05**