Bismillahir Rahmanir Rahim

International Islamic University Chittagong

Department of Computer Science & Engineering

B. Sc. in CSE Semester Final Examination, Spring 2022

Course Code:CSE 3521 Course Title: Computer Architecture

Total marks: 50 Time: 2.5 hours

[Answer all the questions; Separate answer script must be used for **Group-A** and **Group-B**.]

Group-A

1.a)	What are the basic elements in an MIPS data path implementation?	3	CO1
b)	Suppose you are given an instruction sub $s2,$t2,$t3. Describe the complete operation of the datapath using the instruction with a figure.	4	CO1
c)	Why a single-cycle implementation is not used? justify the answer	3	CO2
a)	Design a single cycle data path for handling R-type instruction of MIPS.	3	CO1
b)	Describe all temporary register and multiplexors of Multicycle Datapath	4	CO2
c)	Do you think that the functions of memory data register and instruction register are the same? If not then how?	3	CO3
	Or,		
2. a)	Are instruction and microinstruction same? If not then why?	3	CO1
b)	Illustrate the following instruction with three bus and two bus CPU system and explain which is better? ADD R3, R2, R1	4	CO2
c)	Set the control words for the following microinstructions: i) SUB R1, R2, R0, ii) MAR← PC	3	CO3

Group-B

3.a)	Does any Pipeline Stall arise here for the following instructions, explain:
	MUL R1, R2, R3
	SUB R3, 1, R4
	ADD R4, R5, R6
		4	CO2

b)	Which is advantageous between sequential processing and pipeline processing, explain?	2	CO2
	How does data dependency effect in pipelining?	4	CO2
4.a)	Suppose you have 6 I/O devices in your computer. An output operation will be performed to the Device 4 (could be the keyboard) in the case of shared I/O arrangement. Explain with diagram how the operation will be performed.	5	CO3
b)	Suppose you would like to bi-pass the CPU to perform a job. How a DMA can work in this regard?	5	CO1
5.a)	What is DMA controller? Describe the working principle of DMA controller.	3	CO1
b)	What is TLB? How can you reduce page fault explain logically?	3	CO3
c)	Write short note on handshaking protocol.	4	CO1
	Or,		
5a)	Write short note on memory hierarchy.	3	CO1
b)	Define *cache hit, cache miss, hit rate, tag* in caching.	4	CO1
c)	Suppose you would like to bi-pass the CPU to perform a job. How a DMA can work in this regard ?	3	CO3