International Islamic University Chittagong (IIUC)

Department of Electronic and Telecommunication Engineering

Mid-Term Examination

Program: B.Sc (Engg.) | **Semester: Autumn2022**

Course Code: ETE-4827/4847 | **Course Title: VLSI SYSTEM DESIGN & MODELING**

Total Marks: 30 | **Time-1.5 Hours**

Course Outcomes (COs) of the Questions	
CLO1	Identify and understanding the basic knowledge of VLSI technology and Circuit.
CLO2	Recognize and illustrate the theoretical knowledge of MOS circuit device design and fabrication.
CLO3	Apply and Analyze the knowledge to design different sequential and combinational login circuit using NMOS, PMOS and CMOS.

Bloom's Levels of the Questions						
Letter Symbols	R	U	Ap	An	E	C
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

1. a)	State Moor's Law. Explain the importance of VLSI system and VLSI design methodologies.	5	R, U	CLO1
b)	Sketch the VLSI design Cycle and Briefly describe the following VLSI design cycle i) System specification ii)Architectural design iii) Functional design	5	U	CLO2
2. a)	Explain the threshold voltage characteristic curve of nMOS and pMOS transistor.	5	An	CLO2
b)	Describe the operation of NMOS inverter and explain Voltage transfer characteristic (VTC) curve of NMOS inverter.	5	An	CLO2
	OR			
2. a)	Sketch VTC curve of NMOS resistive load inverter and deduce the equation V_{OH} and V_{OL} for the above inverter.	5	E	CLO2
b)	Design a resistive load inverter with R_L=1KΩ, such that V_{OL} =0.6v, the enhancement type driver transistor has the following parameters V_{dd}=5V, V_{TO}=1V, γ=0.1$V^{1/2}$, λ=0, $\mu_n C_{OX}$=22$\mu A/V^2$, Identify the I) W/L ratio II) Noise margin	5	C	CLO2
3.a)	Describe the operation of CMOS inverter with appropriate diagram and Sketch the VTC curve.	5	An	CLO2
b)	Briefly explain the propagation delay of CMOS inverter with diagram and discuss how minimize the above delay.	5	An	CLO2