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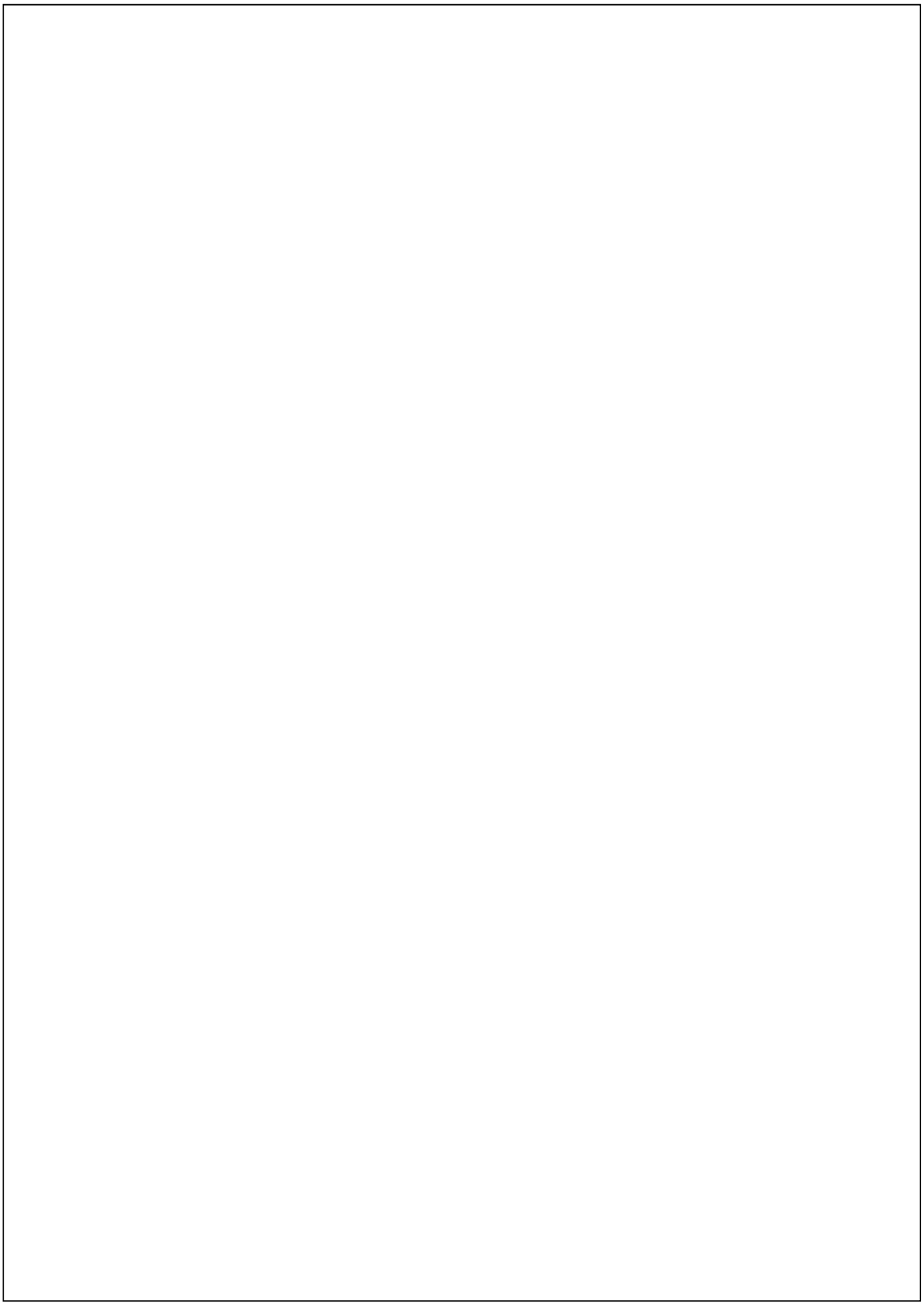

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A thesis
submitted as partial fulfilment of the requirement for the degree of

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CERTIFICATE OF APPROVAL

The thesis entitled as **"A High Speed Dynamic Logic Circuit Design with Low Propagation Delay and Leakage Power for Wide Fan-In Gates"** submitted by **Md. Maharaj Kabir**, bearing Matric ID. **ET181018** and **Fahim Abrar**, bearing Matric ID. **ET181024** of session **Spring 2021**, to the Department of Electrical and Electronic Engineering, International Islamic University Chittagong, has been accepted as satisfactory in partial fulfillment of the requirements for the degree of Bachelor of Science in Engineering and approved for the examination held on **16 April, 2022**.

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DECLARATION

It is hereby declared that this work has been done by us and no portion of the work contained in this thesis/project has been submitted elsewhere for the award of any degree or diploma.

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Md. Maharaj Kabir

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Fahim Abrar

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Authors

ABSTRACT

Dynamic logic circuits are used in higher-functioning circuit applications due to their speed. Once the static logic circuit was used. But it requires a large number of transistors, resulting in a large overhead area and high power consumption. So it is replaced by dynamic logic, which has impressive performance compared to static logic. Dynamic logic circuits are employed in a variety of fields, including microprocessors and dynamic memory, because they are faster and have fewer transistors than static logic circuits. However, it has the leakage power and propagation delay issue, which means it won't be able to demonstrate the necessary performance during the evaluation phase. Wide fan-in domino gates are more compact, resulting in more sub-threshold leakage current channels. When the Pull-Down Network (PDN) is OFF, noise from any source comes at gates and develops a gate to source voltage. It also increases the leakage power and propagation delay. As a result, reducing the leakage power and propagation delay while designing a dynamic logic circuit is a major issue. A novel dynamic logic model with low leakage power and propagation delay in contrast to previous models, is developed by adding delay components and changing stacking effect circuitry. Increased sub-threshold leakage current is one of the primary causes of leakage power rise. Sub-threshold conduction or leakage current is the current that flows between the source and drain of a MOSFET when the transistor is in the sub-threshold region, or weak-inversion region for gate-to-source voltages less than the threshold voltage. When the size of a technical feature is reduced, the supply voltage and threshold voltage are reduced as well. As the threshold voltage drops, the leakage current grows exponentially thus increasing the sub-threshold leakage power. The LTSpice tool is used to illustrate the robustness of the proposed model utilizing 45nm PTM technology for OR-AND logic gate functionality and various supply voltages. Simulation results show a good percentage of improvement in both leakage power and propagation delay.

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LIST OF ABBREVIATIONS

MOS	Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
IC	Integrated Circuit
PDN	Pull-Down Network
PUN	Pull Up Network
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
SPICE	Simulation Program with Integrated Circuit Emphasis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PTM	Predictive Technology Model
HDL	Hardware Description Language
EDA	Electronic Design Automation

CHAPTER 1

INTRODUCTION

1.1 Introduction

The dynamic logic circuit has become popular in the world of electronics. Once upon a time, the static logic circuit was employed. However, a huge number of transistors are required, resulting in a large overhead area and significant power consumption [1]. As a result, it is replaced with dynamic logic, which outperforms static logic. Sizes of CMOS features for VLSI circuit designers, leakage power dissipation has become a top priority. Power dissipation from leakage may develop to dominate total power use. CMOS power consumption is made up of both dynamic and static components. When transistors switch, dynamic power is consumed, and static power is consumed regardless of transistor flipping. Dynamic power consumption was historically (at 180nmătechnology and higher) the single most important worry for low-power chip designers since it accounted for 90% or more of total chip power. As a result, several previously proposed approaches, such as voltage and frequency scaling, were designed to reduce dynamic power. The leakage power has become a significant barrier for existing and future technologies as feature size lowers [2].

Increased sub-threshold leakage power is one of the primary causes of leakage power rise [3]. Sub-threshold conduction, leakage, or drain current is the current that flows between the source and drain of a MOSFET when the transistor is in the sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages less than the threshold voltage. The weak inversion region is another term for the sub-threshold region [4]. When the size of a technical feature is reduced, the supply voltage and threshold voltage are reduced as well. As the threshold voltage drops, the sub-threshold leakage current grows exponentially, increasing the sub-threshold leakage power. Next, in order to improve channel conductivity and performance, the gate oxide, which acts as an insulator between the gate and the channel, should be made as thin as feasible [5]. The phenomenon of sub-threshold leakage of dynamic logic circuit is shown in **Fig. 1.1** below. However, when the gate oxide becomes thinner, the oxide's barrier voltage changes. As a result of the positive gate voltage, some positive charges become trapped in the oxide [6]. As a result, current passes through the oxide. Tunneling current is another name for this

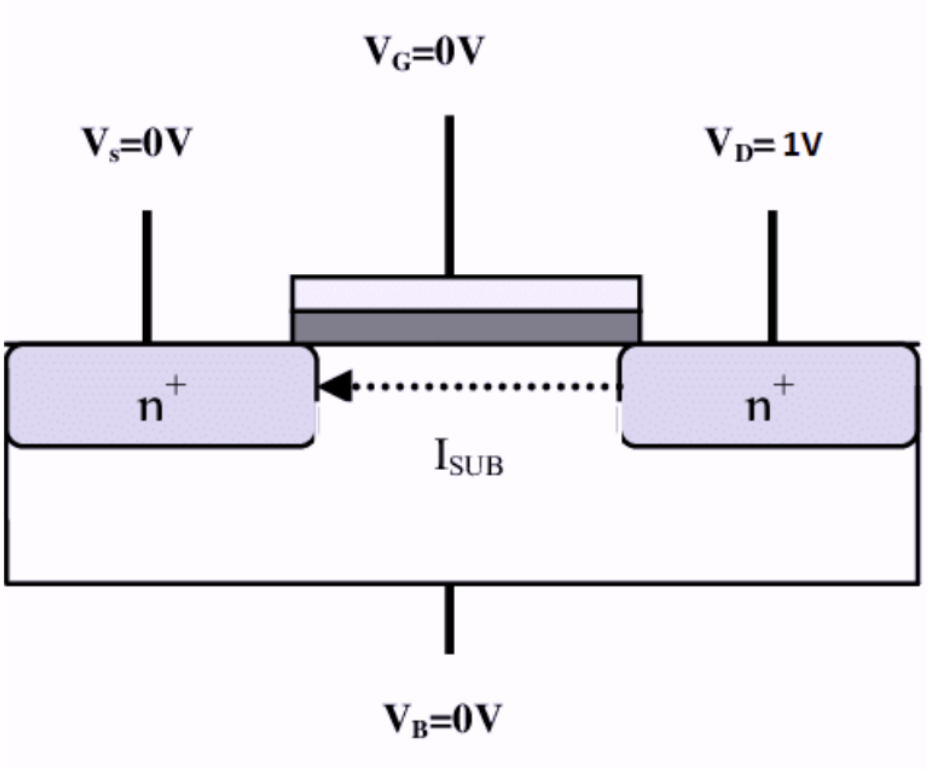

Fig. 1.1 Sub-threshold Leakage of Dynamic Logic Circuit

phenomenon. The propagation delay represents the delay encountered by a signal when traveling through a gate and is defined as how soon it responds to a change at its inputs. The propagation delay is determined as the time between the 50% transition sites of the input and output waveforms. An external clock is used in dynamic logic to examine the circuit operation. The evaluation phase occurs when the clock is logic high. The evaluation step can be divided into two types. The first is that the PDN's inputs are logic low, indicating that the PDN is turned off. Second, the PDN inputs are logic high, indicating that the PDN is active. When the PDN is turned on during the evaluation phase, the dynamic node is discharged fairly through the PDN [7]. When the PDN is turned off during the evaluation phase, however, the dynamic node should maintain the logic high state discovered during the precharge phase. But it doesn't always work out like this. There is always a sub-threshold leakage current through the OFF PDN throughout the evaluation period [8]. The dynamic node is discharged improperly as a result of the leaking current, also causing propagation delay. Wide fan-in domino gates are more

compact, resulting in more sub-threshold leakage current channels. When the PDN is OFF, noise from any source comes at gates and develops a gate to source voltage. It also increases leakage power and propagation delay. This phenomenon is known as crosstalk. As a result, reducing leakage power and propagation delay while designing a dynamic logic circuit is a major issue [9].

1.2 Motivation

Wide fan-in domino gates are more compact, resulting in more sub-threshold leakage current channels. When the PDN is OFF, noise from any source comes at gates and develops a gate to source voltage. It also causes sub-threshold leakage power. This phenomenon is known as crosstalk [10]. So, reducing leakage power is a great challenge while designing a dynamic logic circuit. The dynamic logic circuit has become popular in the world of electronics. Once upon a time, the static logic circuit was employed. However, a huge number of transistors are required, resulting in a large overhead area and significant power consumption. As a result, it is replaced with dynamic logic, which outperforms static logic. In higher-functioning circuit applications, dynamic logic circuits are used because of their speed. However, the dynamic logic's performance isn't very promising due to its propagation delay and leakage current problem. A novel dynamic logic model with low leakage power and propagation delay in contrast to previous models, is developed by adding delay components and changing stacking effect circuitry. The LT-Spice tool is used to illustrate the robustness of the proposed model utilizing 45nm PTM technology and various supply voltages for OR-AND logic gate functionality.

1.3 Thesis Objectives

Since higher contention time and sub-threshold leakage power of domino logic circuit is a problem for the protection of the system, our main goal is to reduce this high propagation delay and sub-threshold leakage power of high performance domino logic circuit. A novel dynamic logic circuit design with very low leakage power and propagation delay is proposed in this thesis. The primary objectives of this thesis is stated below-

1. Designing a domino model which consists of a pull-down network, delay elements, keeper device and stacking effect circuitry.
2. Observing the circuit leakage power and propagation delay for wide fan-in gates in evaluation phase.

3. Observing the circuit performance for wide fan-in logical OR-AND operation.

1.4 Thesis Layout

This thesis is arranged in the following order.

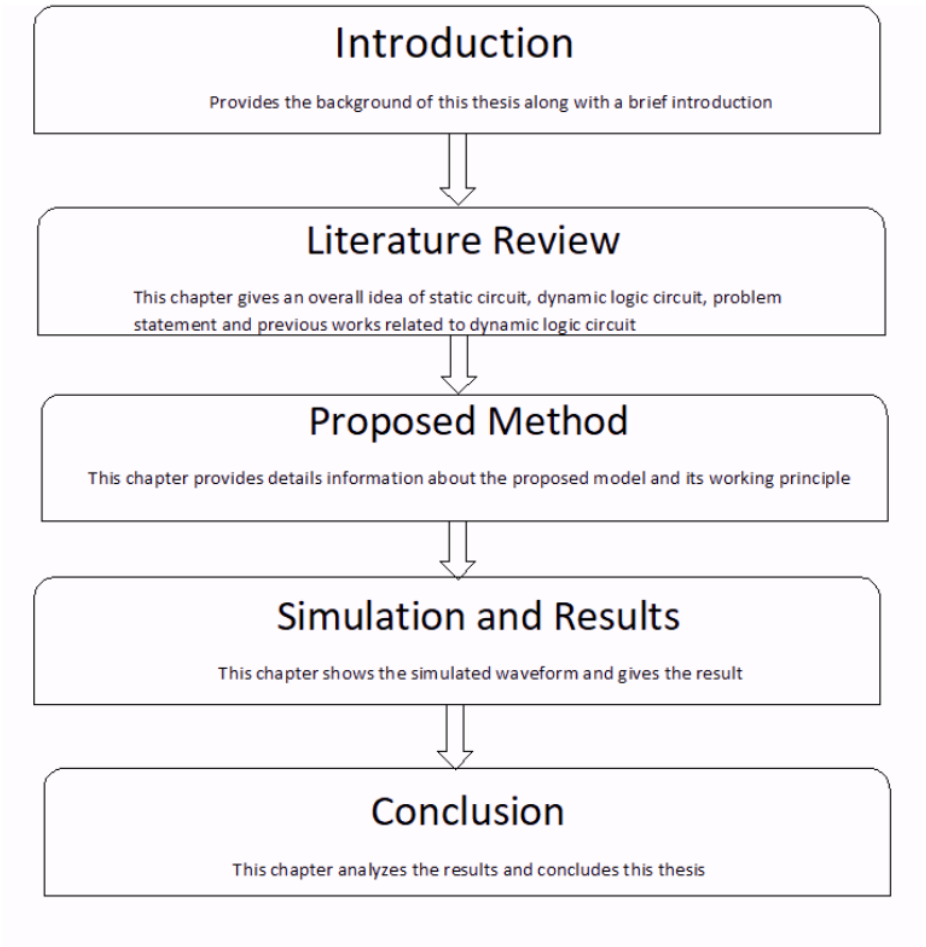

Fig. 1.2 Thesis Layout

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, we will try to give a brief discussion about dynamic CMOS circuit including its basic components, problem statement and previous works to solve the leakage power and propagation delay issue.

2.2 MOS

Metal oxide semiconductor (MOS) represents a category of distinctive materials as a result of their charge transport properties. They distinguish themselves from standard valence semiconductors within which the interaction between the metal and compound orbitals ends up in important inequality of the charge carrier transport. Metal oxides are often doped into either n- or p-type physical phenomenon. They will even be heavily doped to act as conductors with terribly low electrical resistance, a number of that referred to as the clear semiconductive oxides. In metal compound semiconductor, the fabric characteristics, band structure, defects, impurity doping, and electrical properties of some necessary n-type (Indium compound, Zinc oxide, Tin(IV) compound) and p-type (Copper oxide, Nickel compound, Tin(II) oxide) metal oxides ar shortly introduced.In metal-oxide-semiconductor (MOS) transistors, an identical conception applies, however the operational frequency is usually determined by the space between the supply and drain.

The source and drain of an n-channel MOS (NMOS) transistor, for example, are two n-type areas formed in a piece of p-type semiconductor, commonly silicon. The whole semiconductor surface is coated by an insulating oxide layer, with the exception of the two locations where metal leads touch these areas. The metal gate, which is commonly aluminum, is deposited on top of the oxide layer, slightly above the source-drain gap. The semiconductor material behind the gate will have extra holes if no voltage (or a negative voltage) is applied to it, and very few electrons will be able to bridge the gap since one of the two p-n junctions would obstruct their route. As a result, except for inevitable leakage currents, no current will flow in this setup. If the gate voltage is positive, an electric field will penetrate the oxide layer and draw electrons into the silicon layer right behind the

gate (commonly referred to as the inversion layer). When this voltage reaches a certain level, electrons will flow freely between the source and drain. The transistor is switched on.

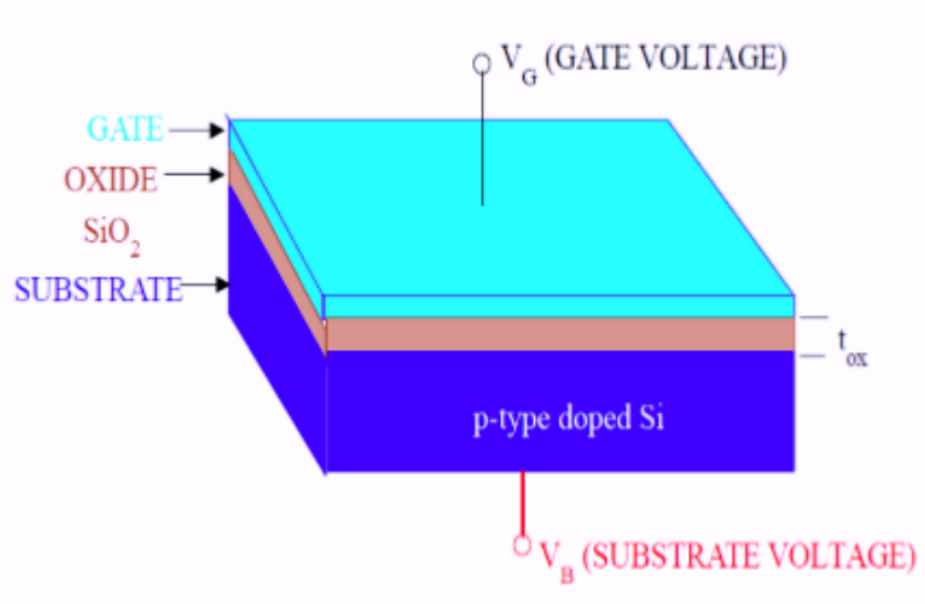

Fig. 2.1 Metal Oxide Semiconductor

A p-channel MOS transistor, in which the source and drain are p-type areas generated in n-type semiconductor material, exhibits similar characteristics. A negative voltage applied over a threshold causes a layer of holes (rather than electrons) to form beneath the gate, allowing a current to flow from source to drain. The operating frequency of n-channel and p-channel MOS (also known as NMOS and PMOS) transistors is mostly determined by the speed with which electrons or holes may wander through the semiconductor material divided by the distance between source and drain. Because electrons have nearly three times the mobility of holes through silicon, NMOS transistors can function at far higher frequencies than PMOS transistors. Smaller distances between source and drain are also conducive to high-frequency operation, and much work has gone into minimizing this gap.

In the 1960s, Fairchild Semiconductor's Frank Wanlass realized that combining an NMOS and a PMOS transistor in standby mode would draw very little currentjust the minuscule, inevitable leakage currents. Only when the gate voltage surpasses a certain threshold and a current flows from source to drain do these CMOS (complementary metal-oxide-

semiconductor) transistor circuits waste considerable power. As a result, they may operate at extremely low power levels, typically a million times lower than bipolar junction transistors. This property of CMOS transistors, along with their intrinsic simplicity of construction, has made them the ideal option for producing microchips, which now squeeze millions of transistors onto a surface area smaller than a fingernail. The waste heat created by the component's power consumption must be reduced to a bare minimum in these instances, otherwise the chips may just melt.

2.2.1 CMOS

Complementary metal oxide semiconductor (CMOS), also known as complementary-symmetry metaloxidesemiconductor (COS-MOS), is a MOSFET production technique that employs complementary and symmetrical pairings of p-type and n-type MOSFETs to perform logic tasks. Microprocessors, microcontrollers, memory chips, and other digital logic circuits are all built using CMOS technology. Image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers are all examples of analog circuits that employ CMOS technology.

In 1959, Mohamed M. Atalla and Dawon Kahng created the MOSFET at Bell Labs, and in 1960, they proved the manufacturing techniques for PMOS (p-type MOS) and NMOS (n-type MOS). Chih-Tang Sah and Frank Wanlass of Fairchild Semiconductor eventually merged and modified these methods into the complementary MOS (CMOS) technology in 1963. In the late 1960s, RCA marketed the technology under the trademark "COS-MOS," requiring other manufacturers to come up with a new moniker, which led to "CMOS" being the industry standard by the early 1970s. In the 1980s, CMOS supplanted NMOS as the primary MOSFET fabrication technique for very large-scale integration (VLSI) circuits, as well as older transistortransistor logic (TTL) technologies. Since then, CMOS has been the industry standard for MOSFET semiconductor devices in VLSI chips. As of 2011, CMOS technology was used to create 99 percent of IC chips, including the majority of digital, analog, and mixed-signal ICs.

High noise immunity and low static power consumption are two significant properties of CMOS electronics. Because one of the MOSFETs in the pair is permanently off, the series combination only drains substantial power while switching between on and off states [11]. As a result, CMOS devices generate less waste heat than other types of logic, such as NMOS or transistortransistor logic (TTL), which have some standing current

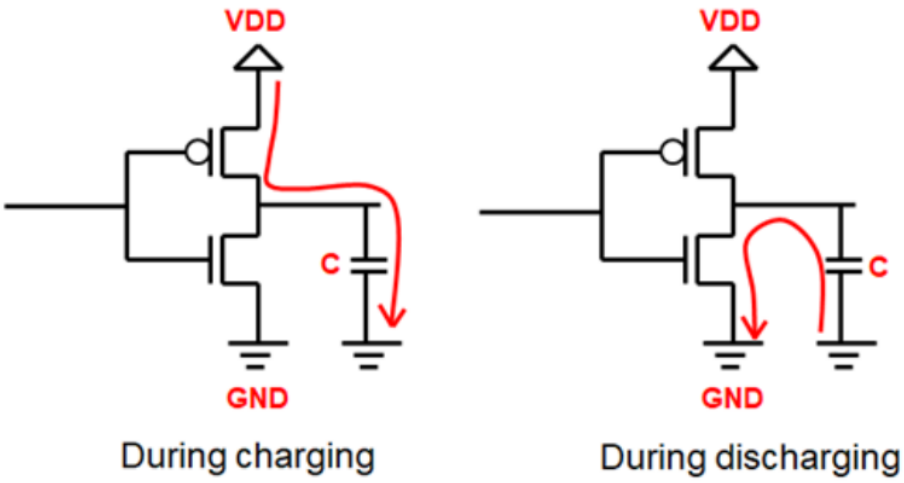

Fig. 2.2 Normal Operation of a CMOS

even when not changing state. Because of these properties, CMOS can fit a lot of logic functions on a single chip. CMOS became the most extensively utilized technology in VLSI chips largely because of this.

The physical structure of MOS field-effect transistors with a metal gate electrode on top of an oxide insulator, which is then on top of a semiconductor material is referred to as metal oxide semiconductor. Previously, aluminum was utilized, but today polysilicon is used. With the introduction of high-dielectric materials in the CMOS process, other metal gates have made a comeback, as reported by IBM and Intel for the 45 nm node and lower sizes. The term "CMOS" refers to both a type of digital circuit architecture and a set of technologies for putting such circuitry on integrated circuits [12]. The power dissipated by CMOS circuitry is lower than that of logic families with resistive loads. Since this advantage has risen in importance, CMOS processes and variations have come to dominate, with CMOS technologies accounting for the great majority of current integrated circuit manufacture. CMOS logic uses roughly 100,000 times less power than bipolar transistor-transistor logic and about 7 times less power than NMOS logic (TTL). To build logic gates and other digital circuits, CMOS circuits combine p-type and n-type metaloxidesemiconductor fieldeffect transistors (MOSFETs). Although separate devices can be used to demonstrate CMOS logic, commercial CMOS products are integrated circuits containing billions of both types of transistors on a rectangular piece of silicon measuring between 10 and 400 square millimeters. All enhancement-mode MOSFETs

are always used in CMOS (in other words, a zero gate-to-source voltage turns the transistor off).

2.3 VLSI

The technique of producing an integrated circuit (IC) by merging thousands of transistors into a single chip is known as very large scale integration (VLSI). When sophisticated semiconductor and communication technologies were being developed within the Seventies, VLSI was born. A VLSI device is used as the microprocessor [13]. Prior to the development of VLSI technology, most ICs could only execute a restricted range of functions. A CPU, ROM, RAM, and other glue logic may be found in an electrical circuit. VLSI allows IC designers to combine all of these functions into a single chip. Moore's rule states that the number of transistors per silicon chip doubles every year, as predicted by American engineer Gordon Moore in 1965.

The physical science sector has adult at a unsafe pace in recent decades, due to quick developments in large-scale integration technologies and system style applications. The number of IC applications in high-performance computing, controls, telecommunications, image and video processing, and consumer electronics has been rapidly increasing since the introduction of VLSI designs [14]. End-users benefit from today's cutting-edge technologies, such as high-resolution, low-bit-rate video and cellular communications, which offer a vast array of applications, processing power, and mobility. This tendency is projected to accelerate, with significant ramifications for VLSI and systems design. The many design stages are labeled, and the blocks depict design processes.

The specifications come first, and they specify the functionality, interface, and architecture of the digital IC circuit to be constructed in abstract terms. The design is subsequently analyzed in terms of functionality, performance, compliance with provided standards, and other criteria using a behavioral description. HDLs are used to describe Register-Transistor Level. To test practicality, this Register-Transistor Level description is emulated. From here on out, we'll want the help of EDA tools. Logic synthesis tools area unit then wont to rework the Register-Transistor Level description to a gate-level netlist. A gate level netlist could be a illustration of the circuit in terms of gates and connections between them, designed to match the temporal arrangement, power, and space needs [15].

After that, a physical layout is created, which is then confirmed before being submitted to

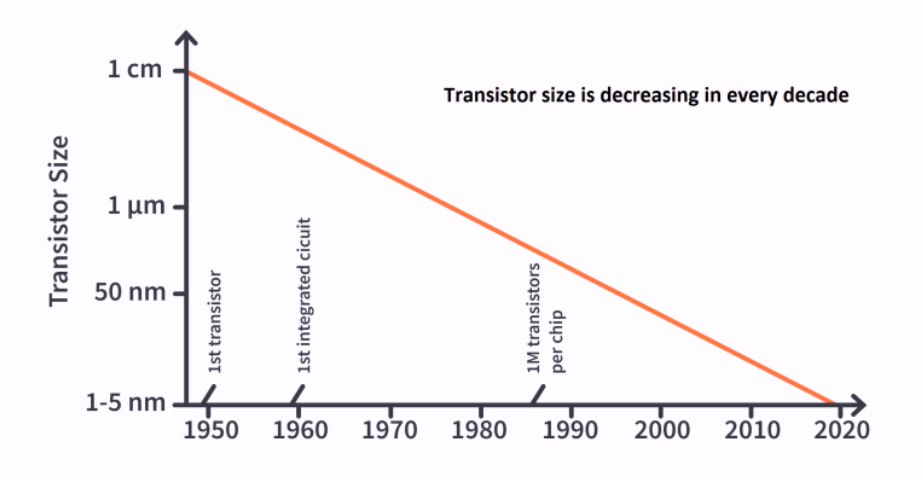

Fig. 2.3 Observation of Moore's law in VLSI design

manufacture. On a single PCB, electrical circuits often include a CPU, RAM, ROM, and other peripherals. VLSI technology, on the other hand, allows an IC designer to combine all of these functions into a single chip. We can detect indications of fast expansion in the electronics scene over the previous few decades if we go back far enough. Increased functionality, miniaturization, and overall performance are among the advantages. However, the desire to install more components while using less space means that the margin for error is shrinking. With this in mind, it's easy to see why Silicon (CMOS) technology has become the dominating manufacturing technique for cost-effective and reasonably high-performance VLSI circuits in recent years.

The technique of embedding or integrating hundreds of thousands of transistors onto a single silicon semiconductor microchip is known as very large-scale integration. VLSI technology was first developed in the late 1970s, about the same time as high level processor (computer) microchips were being developed. Microprocessors and micro controllers are two of the most prevalent VLSI devices. VLSI is a type of integrated circuit that has several devices on a single chip. The word, like many other scale integration classifications based on the number of gates or transistors per IC, dates back to the 1970s.

The advancements in large-scale integration technologies are principally responsible for the electronics industry's extraordinary growth. The number of options for ICs in control applications, telecommunications, high-performance computing, and consumer electronics as a whole continues to grow with the emergence of VLSI designs. Due to VLSI tech-

nology, today's technologies such as smartphones and cellular communications provide unparalleled mobility, processing capacity, and application access. As demand continues to rise, the projection for this trend implies a quick growth. In general, VLSI IC design consists of two main stages or parts:

Digital design employing a hardware description language, such as Verilog, System Verilog, or VHDL, is referred to as front-end design. Additionally, design verification using simulation and other verification techniques is included at this step. Designing, which begins with the gates and goes through to design for testability, is also part of the process. Characterization and CMOS library design are included in the back-end design. It also includes physical design and failure simulation.

The complete design process is organized in a step-by-step manner, including the following front-end design steps:

Problem Specification: This is a system's high-level interpretation. We look at design methodologies, functionality, performance, manufacturing technology, and physical dimensions, among other things. The VLSI system's final requirements include its power, functionality, speed, and size.

Architecture Definition: This comprises basic characteristics like floating-point units, which system to use, and the cache size of the ALU.

Functional Design: This identifies a system's critical functional components and allows for the identification of each unit's physical and electrical specifications, as well as connecting needs.

Logic Design: Control flow, Boolean expressions, word width, and register allocation are all part of this stage.

Circuit Design: This step completes the circuit realization in the form of a netlist. Because this is a software stage, the output is checked using simulation.

Physical Design: By transforming the netlist into a geometrical representation, we can now design the layout. This stage also adheres to some predetermined static criteria, such as the lambda rules, which provide precise ratio, component spacing, and size information.

The following are the back-end design steps for hardware development:

Wafer Processing: In this stage, pure silicon is melted in a saucepan at 1400 degrees Celsius. A tiny seed containing the necessary crystal orientation is then introduced into

liquid silicon and slowly drawn out at 1mm per minute. Before polishing and crystal alignment, we make the silicon crystal as a cylindrical ingot and cut it into discs or wafers.

Lithography: Masking with photo etching and a photographic mask are used in this procedure (photolithography). The wafer is then covered in a photoresist coating. The wafer is then aligned to a mask using a photo aligner. Finally, the wafer is exposed to ultraviolet light to highlight the tracks visible through the mask.

Etching: To make patterns, we remove material from the wafer's surface selectively. We utilize more plasma or chemicals to remove the leftover photoresist after protecting the vital areas of the material with an etching mask.

Ion Implantation: In this case, we use a procedure of introducing dopants to obtain a desired electrical characteristic in the semiconductor. A beam of high-energy dopant ions is used to target specific portions of the wafer in this procedure. The depth of wafer penetration is determined by the energy level of the beam.

Metallization: We apply a thin coating of aluminum to the whole wafer in this phase.

Assembly and Packaging: Hundreds of chips are packed inside each wafer. As a result, we cut the wafers into single chips with a diamond saw. They are then electrically tested, and any failures are discarded. Those who pass, on the other hand, are subjected to a full visual examination under a microscope. Finally, we package and review the chips that pass the visual examination.

VLSI technology is ideally suited to the demands of today's electronic devices and systems. With the ever-increasing demand for shrinking, movability, performance, dependableness, and practicality, VLSI technology can still drive natural electronics advancement.

2.3.1 Static Logic

Static logic is consists of PMOS and NMOS. If we want to observe any logical operation, we need to design PUN and PDN which are consist of PMOS and NMOS respectively. It increases the overhead area of CMOS, propagation delay, leakage power. But there are some benefits in static CMOS also. It offers no lead-lag issue or RACE problem in circuits. Moreover static CMOS has no fault state or invalid state at output which often occurs in dynamic CMOS. Static CMOS is a logic circuit design type in which the output is always aggressively pushed since it is always connected to either V_{CC} or GND (except

when switching) [16].

2.3.2 Dynamic Logic

The dynamic logic circuit has earned an attraction in the field of electronics. Once the static logic circuit was used.ăBut it requires a large number of transistors, resulting in a large overhead area and high power consumption. So it is replaced by dynamic logic, which has impressive performance compared to static logic [17].

Fig. 2.4 depicts a basic dynamic logic. It depicts a footless domino logic circuit with a 4-bit OR logic gate. At the source of the precharge device PMOS transistor Mp, a power supply (Vdd) is applied. To observe the real circuit operation, a clock is applied to Mp's gate. The Mp and pull-down transistors' drains are connected to the dynamic node (NMOS). Inputs in all gates of the pull-down network (PDN) are labeled IN1, IN2, IN3, and IN4 as it is a 4-bit OR logic gate. At the dynamic node, an inverter is added, resulting in domino logic. The precharge phase occurs when the clock is low, after which Mp switches on and the dynamic node becomes logic high. It is now called the evaluation phase when the clock is logic high. If any input of the PDN is logic high during the evaluation phase, the PDN is turned on, and the dynamic node is fairly discharged through the network. Furthermore, the dynamic node should preserve the logic high status identified during the precharge phase if the PDN is switched off during the evaluation phase. However, this isn't always the case. There is always a sub-threshold leakage current through the OFF PDN throughout the evaluation period. The dynamic node is discharged improperly as a result of the leaking current, also causing propagation delay. Dynamic logic circuits, on the other hand, are employed in a variety of fields, including microprocessors and dynamic memory, because they are faster and have fewer transistors than static logic circuits. However, it has a leakage current and propagation delay issue, which means it won't be able to demonstrate the necessary performance during the evaluation phase [18].

The dynamic logic circuit has earned an attraction in the field of electronics. Once the static logic circuit was used.ăBut it requires a large number of transistors, resulting in a large overhead area and high power consumption. So it is replaced by dynamic logic, which has impressive performance compared to static logic [19]. As a result, it is replaced with dynamic logic, which outperforms static logic. Sizes of CMOS features For VLSI circuit designers, leakage power dissipation has become a top priority. Power

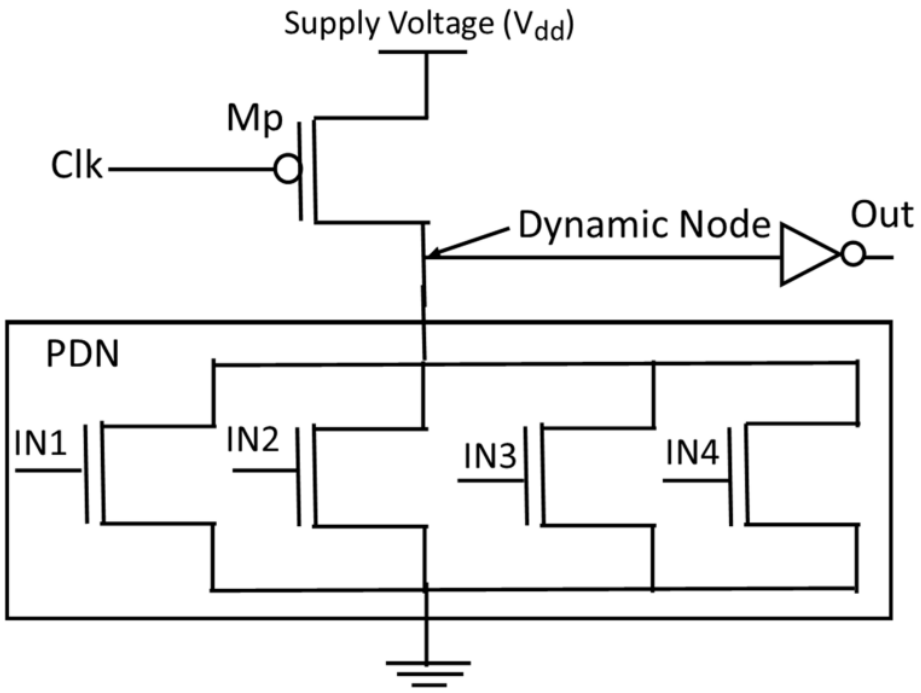

Fig. 2.4 Basic Domino Logic

dissipation from leakage may develop to dominate total power use. CMOS power consumption is made up of both dynamic and static components. When transistors switch, dynamic power is consumed, and static power is consumed regardless of transistor flipping. Dynamic power consumption was historically (at 180nmătechnology and higher) the single most important worry for low-power chip designers since it accounted for 90% or more of total chip power. As a result, several previously proposed approaches, such as voltage and frequency scaling, were designed to reduce dynamic power. Static power, on the other hand, has become a significant barrier for existing and future technologies as feature size lowers. Increased sub-threshold leakage power is one of the primary causes of leakage power rise. Sub-threshold conduction, leakage, or drain current is the current that flows between the source and drain of a MOSFET when the transistor is in the sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages less than the threshold voltage. The weak inversion region is another term for the sub-threshold region. When the size of a technical feature is reduced, the supply voltage and threshold voltage are reduced as well. As the threshold voltage drops, the sub-threshold leakage current grows exponentially, increasing the sub-threshold leakage power. Next, in or-

der to improve channel conductivity and performance, the gate oxide, which acts as an insulator between the gate and the channel, should be made as thin as feasible.

When the gate oxide becomes thinner, the oxide's barrier voltage changes. As a result of the positive gate voltage, some positive charges become trapped in the oxide. As a result, current passes through the oxide. Tunneling current is another name for this phenomenon. The propagation delay represents the delay encountered by a signal when traveling through a gate and is defined as how soon it responds to a change at its inputs. The propagation delay is determined as the time between the 50% transition sites of the input and output waveforms. An external clock is used in dynamic logic to examine the circuit operation. The evaluation phase occurs when the clock is logic high. The evaluation step can be divided into two types. The first is that the PDN's inputs are logic low, indicating that the PDN is turned off. Second, the PDN inputs are logic high, indicating that the PDN is active. When the PDN is turned on during the evaluation phase, the dynamic node is discharged fairly through the PDN. When the PDN is turned off during the evaluation phase, however, the dynamic node should maintain the logic high state discovered during the precharge phase. But it doesn't always work out like this. There is always a sub-threshold leakage current through the OFF PDN throughout the evaluation period. The dynamic node is discharged improperly as a result of the leaking current, also causing propagation delay. Wide fan-in domino gates are more compact, resulting in more sub-threshold leakage current channels. When PDN is OFF, noise from any source comes at gates and develops a gate to source voltage. It also increases leakage current and propagation delay. This phenomenon is known as crosstalk. As a result, reducing leakage current and propagation delay while designing a dynamic logic circuit is a major issue.

2.3.2.1 Leakage Power

The main reason for the widespread use of CMOS technology is to save energy. However, when the size of the technological feature shrinks, the sub-threshold leakage current increases as the threshold voltage decreases. This design criteria emphasizes sub-threshold leakage power consumption, as well as body biasing and stacking effects. Finally, we go through the general CMOS circuit's switching power and propagation delay.

There are three types of power dissipation in CMOS:

1. Dynamic power is dissipated only when switching.

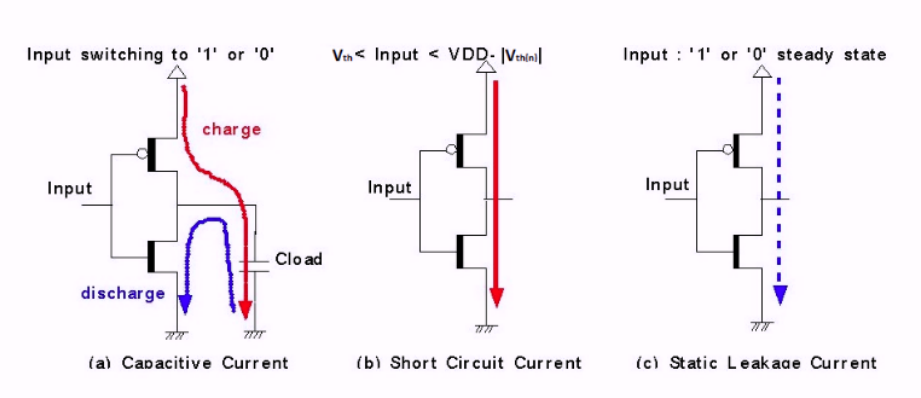

Fig. 2.5 Leakage Power of Dynamic Logic Circuit

2. Leakage current is permanent and results in a continuous loss.

3. Short circuit current loss.

Total power dissipation in CMOS, $P_{total} = P_{switching} + P_{short-circuit} + P_{Leakage}$

Sub-threshold leakage current, $I_{Leakage} = \mu_0 C_{ox}(W/L_{eff})V_\theta^2 e^{1.8} e^{\frac{(-V_{th0}+\eta V_{dd})}{nV_\theta}}(1 - e^{\frac{-V_{ds0}}{V_\theta}})$

Where,

$P_{short-circuit} = t_{sc} * V_{DD} * I_{sc}$

$P_{switching} = C_{Load} * (V_{DD}^2) * f$

$P_{Leakage} = V_{DD} * I_{leakage}$

t_{sc} = CMOS short circuit time

V_{DD} = Supply Voltage

C_{Load} = Load capacitance

V_θ = Thermal Voltage

n = sub-threshold coefficient

I_{sc} = short circuit current from PMOS to NMOS

V_{th0} and V_{ds0} are the the zero-bias threshold voltage, the drain to source voltage respectively. γ is the body bias effect coefficient, and η is the drain induced barrier lowering coefficient. μ is zero bias mobility, C_{ox} is the gate oxide capacitance, W is the transistor width, and L_{eff} is the effective channel length. we assume $\mu_n = 2\mu_p$, as hole mobility is almost 2 times slower than electron mobility.

$P_{switching}$ denotes the power consumed by logic gates as a result of charging and discharging circuit capacitances. During output voltage changes, $P_{short-circuit}$ represents the short circuit current flowing from V_{DD} to ground. Scaling down technology and increasing temperature substantially affect leakage power $P_{Leakage}$, which is extremely important for reducing leakage power in dynamic logic circuits.

Threshold Voltage, $V_{th} = V_{t0} + \gamma(\sqrt{V_{sb}})$

V_{t0}= Threshold Voltage at zero temperature

γ= body bias effect coefficient

V_{sb}= body to source voltage

The body bias effect can be used to adjust the threshold voltage. The threshold voltage changes as the substrate voltage changes. As a result, numerous types of effects emerge when the substrate voltage is changed, such as zero body bias, reverse body bias, and forward-body bias. The threshold voltage is routinely controlled using this phenomenon. γ constant is determined by the transistor parameter and the size of the technological feature. We can simply adjust the leakage power by managing the body biasing effect by modifying the constant term.

2.3.2.2 Propagation Delay

The propagation delay of a logic-circuit family's fundamental inverter defines the dynamic performance of the family. The average of the low-to-high t_{PLH} and high-to-low t_{PHL} propagation delays is used to calculate the inverter propagation delay t_P :

$$\frac{t_{PLH} + t_{PHL}}{2}$$

The propagation delays t_{PLH} and t_{PHL} are defined as the time it takes for the output voltage to reach the midpoint of the low and high logic levels, which in our instance is 50% of V_{DD} in CMOS logic. **Fig. 2.6** shows how the propagation delay is defined.

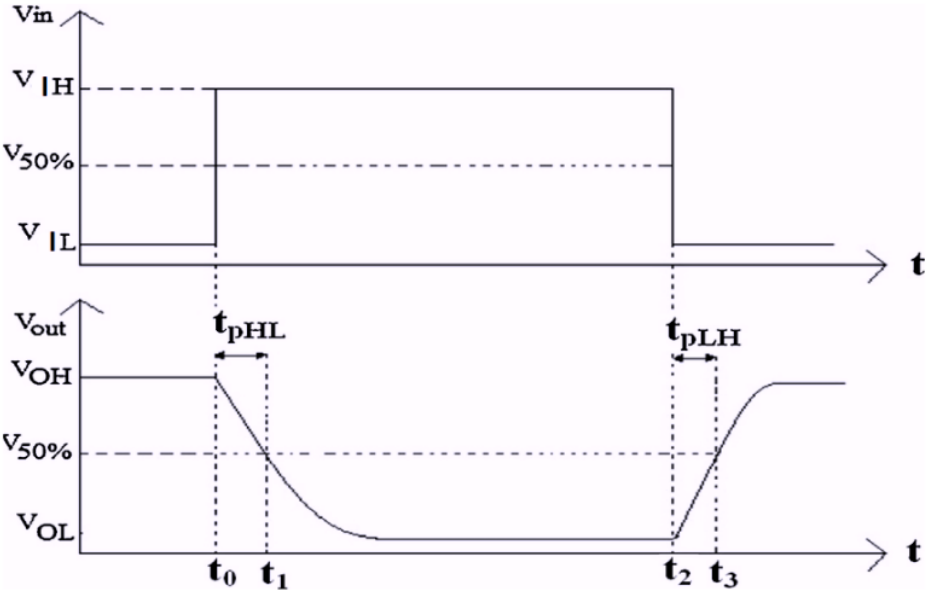

Fig. 2.6 Propagation Delay

2.4 Problem Statement

The propagation delay represents the delay encountered by a signal when traveling through a gate and is defined as how soon it responds to a change at its inputs. The propagation delay is determined as the time between the 50-percent transition sites of the input and output waveforms. An external clock is used in dynamic logic to examine the circuit operation, as shown in **Fig. 2.4**. The evaluation phase occurs when the clock is logic high. The evaluation step can be divided into two types. The first is that the PDN's inputs are logic low, indicating that the PDN is turned off. Second, the PDN inputs are logic high, indicating that the PDN is active. When the PDN is turned on during the evaluation phase, the dynamic node is discharged fairly through the PDN. When the PDN is turned off during the evaluation phase, however, the dynamic node should maintain the logic high state discovered during the precharge phase. But it doesn't always work out like this. There is always a sub-threshold leakage current through the OFF PDN through-out the evaluation period. The dynamic node is discharged improperly as a result of the leaking current, also causing propagation delay.

Wide fan-in domino gates are more compact, resulting in more sub-threshold leakage current channels. When the PDN is OFF, noise from any source comes at gates and develops a gate to source voltage. It also increases the leakage current and propagation

delay. This phenomenon is known as crosstalk. As a result, reducing the leakage power and propagation delay while designing a dynamic logic circuit is a major issue.

2.5 Previous works

Wide fan-in domino gates are more compact, resulting in more sub-threshold leakage power channels. When the PDN is OFF, noise from any source comes at gates and develops a gate to source voltage. It also causes sub-threshold leakage power. This phenomenon is known as crosstalk. So, reducing leakage power and delay is a great challenge while designing a dynamic logic circuit.

Now, we will examine some previously developed models that tried to improve the circuit performance by means of keeper circuits, footer device, stacking effect circuitry, scaling of technology, and weaker keeper device circuitry.

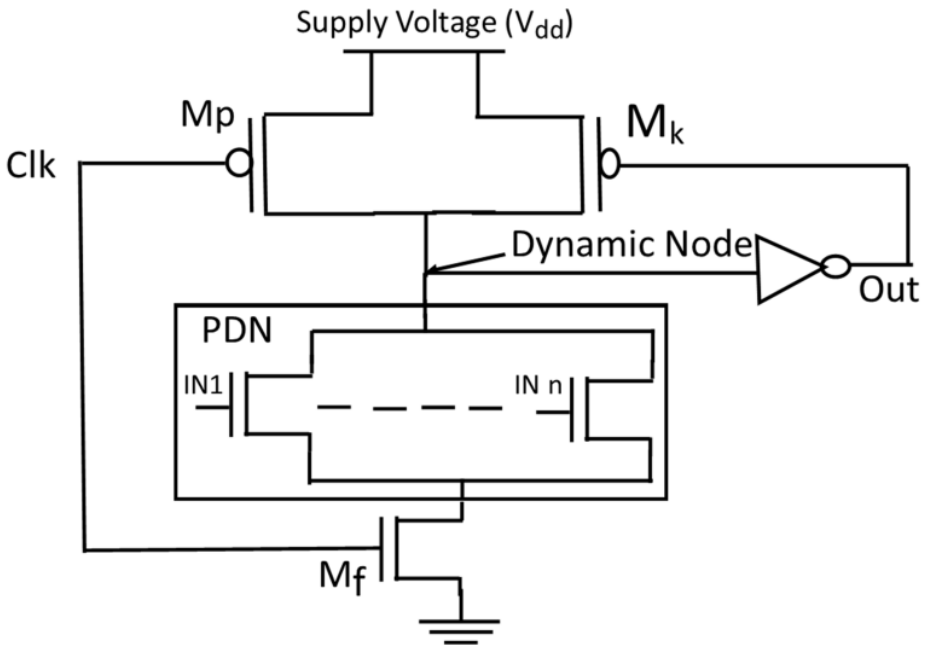

Fig. 2.7 Footer Domino

When the PDN is turned off in the evaluation phase, the fundamental difficulty of a simple dynamic logic circuit is leakage power. A footer NMOS M_f is placed below the PDN, as shown in Fig. 2.7. This slightly reduces the leakage power. When the PDN is turned off in the evaluation phase, a keeper device M_K is introduced to hold the stored charge at the dynamic node. However, during the precharge phase, a precharge device is used to

charge the dynamic node up to V_{DD}.

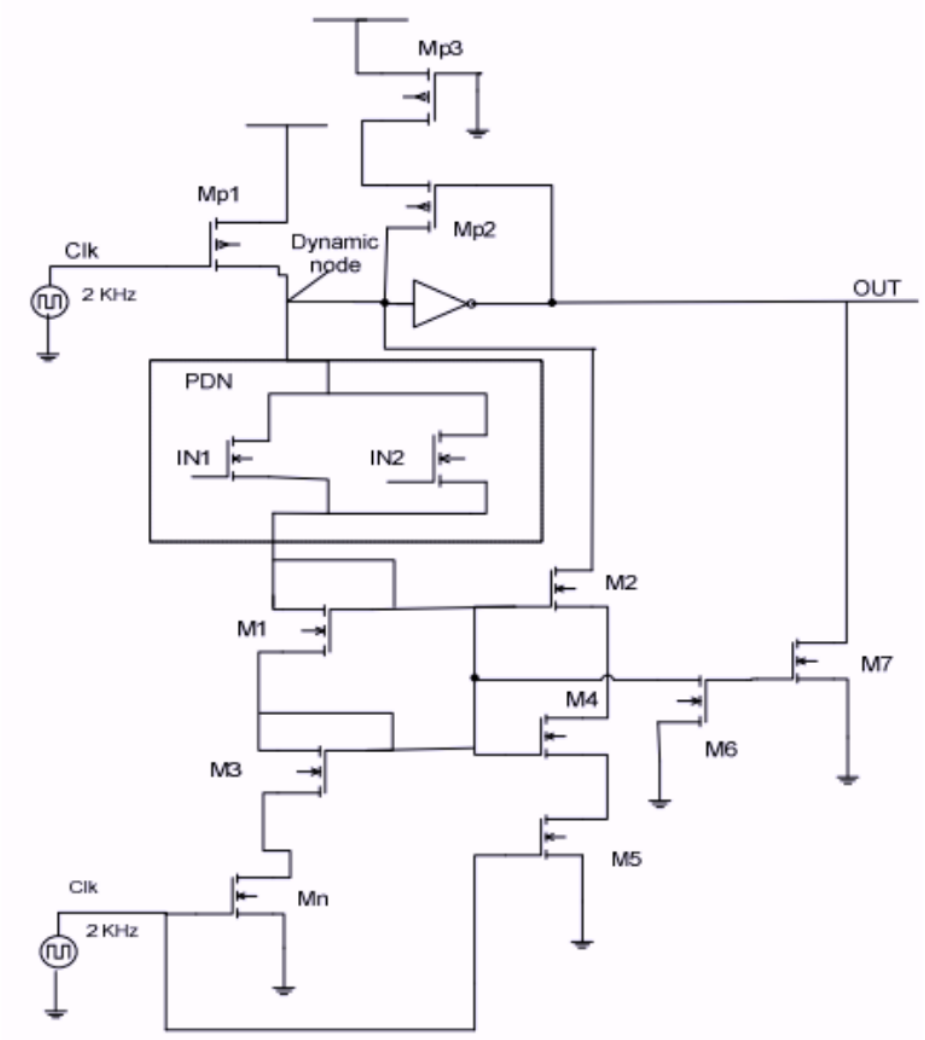

Fig. 2.8 Proposed model of Shiksha et el.

Fig. 2.8 depicts the suggested domino logic architecture of Shikhsa et al. In this design, current mirror circuits are utilized in place of footer transistors in the stack. Current mirror circuits are designed such that any noise signal generated at M1 leaks to ground via M4 and M5. Transistors M3 and M4 also form a current mirror, and the gate to source voltage of the NMOS pull down network lowers fast as a result of both current mirror circuits. The stacking effect is the name for this phenomena. M4 and M5 are used in the proposed circuit to provide a stacking effect, which minimizes the voltage drop across

M2. In the proposed circuit, the existence of current mirrors produces an increase in latency. To address this issue, the PDN's size (W/L ratio) should be raised. The stacking effect causes the circuit to lose power and become less noise resistant. Because of the stacked current mirrors in this proposed circuit, there will be a voltage drop during the assessment phase. The circuit's sub-threshold current will be reduced exponentially due to negative Vgs. In order to enhance the power-delay product even further, the size of the PMOS transistor in the inverter circuit at the output node should be four times that of the NMOS transistor. Because PMOS transistors are utilized to supply strong one logic to circuits, the purpose of transistor Mp3 is to deliver strong Vdd to the lower PMOS Mp2.

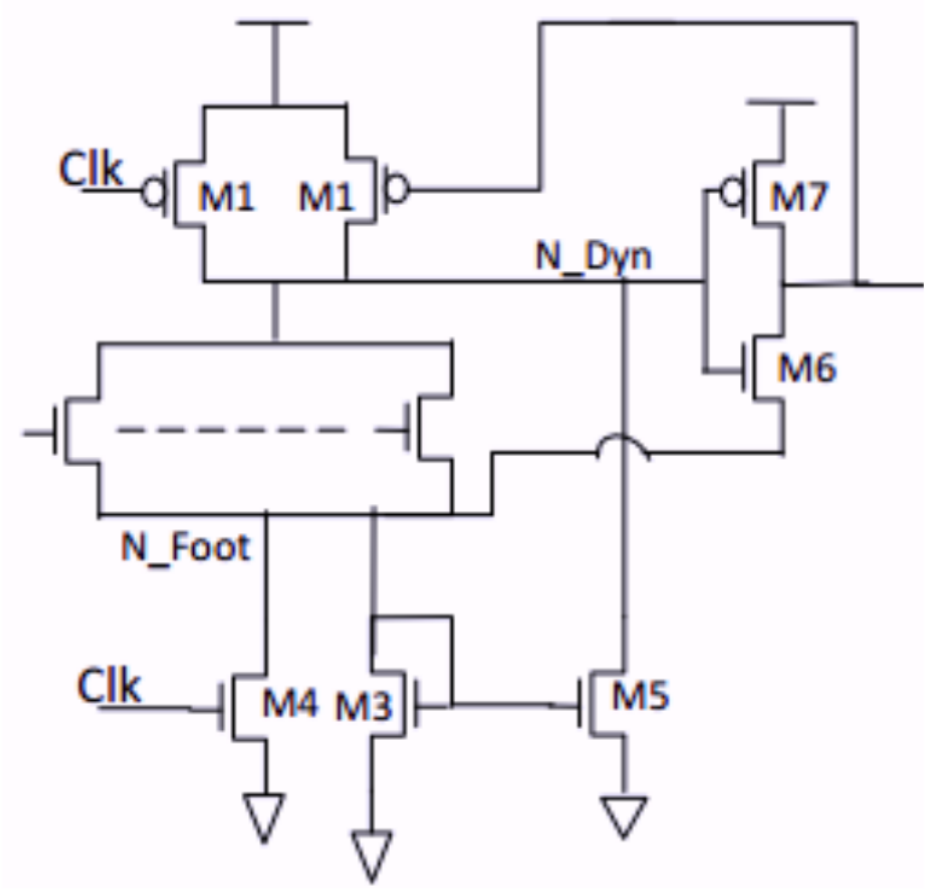

Fig. 2.9 Proposed model of Meher et el.

Fig. 2.9 depicts the suggested domino logic architecture of Meher et al. A diode-footed domino in series with the PDN, a current mirror circuit parallel to the diode foot, and a semidynamic buffer in which the domino logic's buffer is not grounded and is linked to

the PDN foot have all been added to the circuit. The drain and gate terminals of the three transistors are shorted to create the diode footer. Sub-threshold leakage is reduced as a result of the diode footer's stacking effect. During the assessment phase, there is a voltage drop across the diode footer. V_{GS} turns negative as a result of the voltage decrease. The threshold voltage is reduced exponentially as a result of this. The drawback of the diode footer, according to H Mahmoodi et al, is that it raises the switching threshold voltage of the gate by the NMOS threshold, and the new threshold value is roughly $2V_{TN}$ of the original. As a result, the circuit's performance will suffer. After then, the performance deterioration is reduced by using a current mirror that reflects the current. The stream may now be simply drained to the ground.

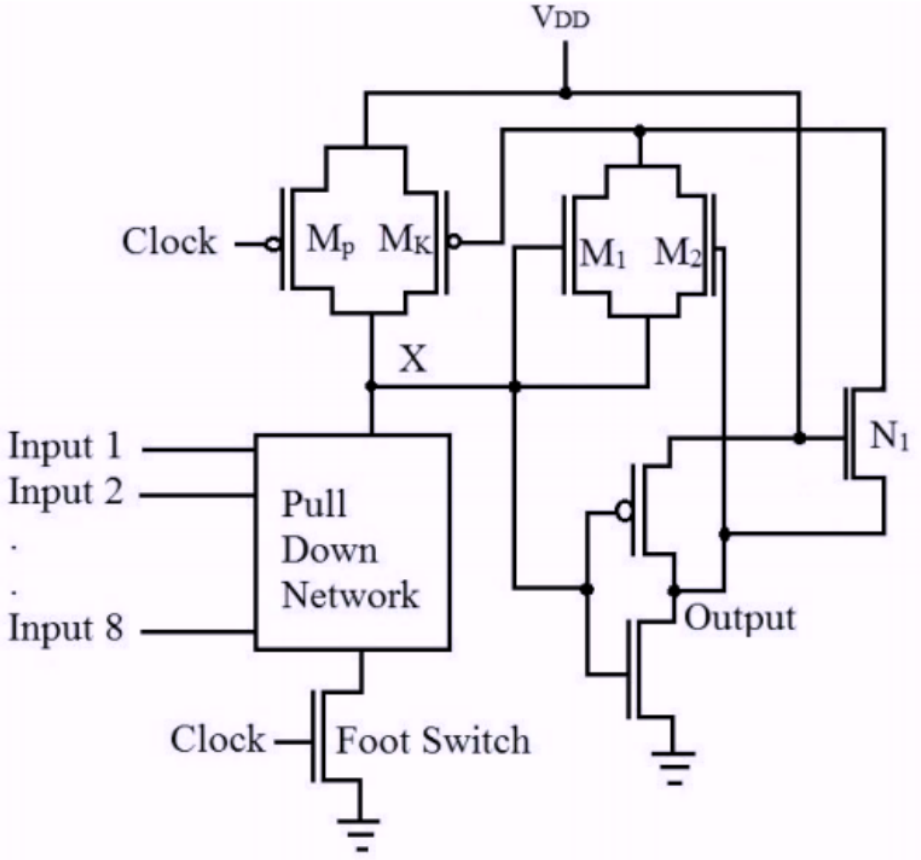

Fig. 2.10 Proposed model of Mahbubul et al.

Fig. 2.10 depicts the suggested domino logic architecture of Mahbubul et al. The keeper gate is connected to the nMOS-based resistive gate in this study. This gate is essentially

made up of two NMOS transistors. Both are linked in a parallel manner, but neither is in an ON state at the same moment. When one NMOS is active, the other is turned off. Both are the same size in terms of length and width. It acts as a resistor in front of the keeper gate. Traditional domino logic has a longer time delay and a lower noise margin, whereas this resistive gate has a shorter time delay and a higher noise margin. The domino node's resistive gate input will alter its value during the precharge and evaluation phases. It shows the entire topology of the NMOS-based resistive gate domino logic, which includes two PMOS Mp and Mk as precharge and keeper devices. Parallel connections are made between two NMOS devices. When the clock is zero during the precharge phase, the dynamic node is in high state and the output is 0. As biased by 0, M1 is on and M2 is off. In the evaluation phase, the clock is set to 1, the dynamic gate is discharged from the PDN, and the output changes from 0 to 1. M2 is currently biased by a high voltage from the output. A NMOS-based resistive gate and a 0 to 1 clock transition generate differential waveforms at the keeper transistor gate at the start of the evaluation phase. As a result, the keeper network is less effective than the pull-down network. Because the keeper device requires a minimum voltage, V_{Gmin} is required. The driving deterioration of the keeper device can be solved by lowering or raising the threshold voltage of the keeper device. The keeper gate will be able to attain zero voltage with this circuit. N1 is included in the design to act as a sub-threshold condition, assisting the resistive gate in completely discharging the keeper gate (if the input combination is "0") and increasing the driving capability of the precharge and keeper transistors. As a result, the noise margin and time delay in domino logic will grow. The wave patterns of resistive gate feedback during the precharge and evaluation phases.

However, the mentioned models tried to improve the circuit performance by means of keeper circuits, footer device, stacking effect circuitry, scaling of technology, and weaker keeper device circuitry. They have improved the noise margin and overhead area parameters of domino CMOS. But, we can observe that the leakage power and propagation delay problems are still significant in these mentioned models.

CHAPTER 3

PROPOSED METHOD

3.1 Introduction

In this thesis, delay elements have been added, and stacking effect circuitry has been modified to reduce leakage current and propagation delay. Here, the operation of the proposed model is briefly defined.

3.2 precharge phase

The proposed dynamic logic design is shown in **Fig. 3.1**. Firstly, the PDN is turned off, and then the OR logic gate operation is performed. The precharge and keeper devices turn on when the clock is low. During the precharge phase, the dynamic node will obtain logic high up to V_{dd}. The NMOS (M5) will not be turned on. The stacking effect circuitry will stay inactive as long as the clock is low. As a result, the logic high state at the dynamic node is preserved.

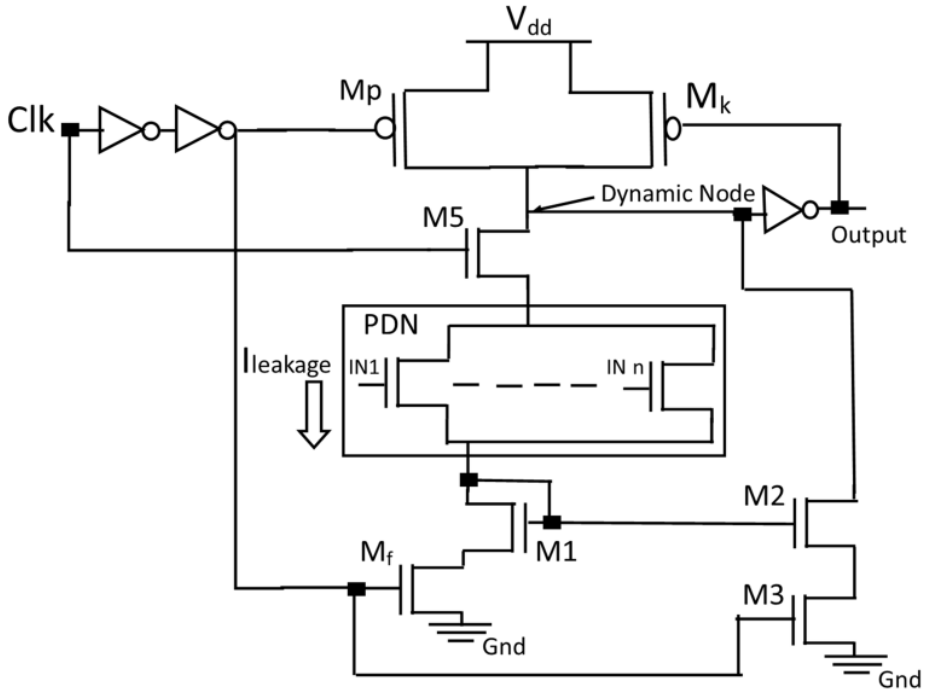

Fig. 3.1 Proposed Dynamic Model

3.3 Evaluation Phase

The dynamic node will attempt to discharge itself through the PDN even if the PDN is turned off at the beginning of the evaluation phase. The delay element was used immediately after the clock. These delay elements, as well as NMOS (M5), are used to limit sub-threshold leakage current across the PDN. The gate of NMOS (M1) is connected to the footer diode NMOS (M1), which has a short gate and drain (M2). A current mirror circuit is created as a result of this. The sub-threshold leakage current through the mirror circuit is limited by the NMOS (M3) below it (M2). The footer transistor (Mf) is employed as usually. A stacking effect is created by the circuitry below the PDN. Even if some leakage current tries to pass through the PDN, the circuitry's stacking effect reduces leakage current. When the PDN is turned off, the suggested model maintains the logic high state at the dynamic node in the evaluation phase.

Now, if any gate of the PDN is set to logic high, the PDN will be turned on. The dynamic node will be fairly discharged to the ground during the evaluation period using the active PDN which is done using the LTSpice tool and 45nm PTM technology. Aside from that, noise at the gate of the PDN causes the gate to source voltages of NMOS in the PDN to rapidly decrease due to the stacking effect. The OR logic gate operation is considered in the PDN. In the proposed model, the width-to-length ratio of NMOS is set at 0.5. The width of PMOS is taken 2 times greater than that of NMOS, as hole mobility is almost 2 times slower than electron mobility. The propagation delay and the leakage power is reduced significantly, which is discussed in the result section. Scaling the threshold voltage of transistors used in the proposed model can reduce the leakage power and propagation delay even more.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Introduction

The proposed model for 8-bit OR logic gate operation with a supply voltage of 1V has been simulated in **Fig. 4.1**, which illustrates the dynamic node versus clock waveform in the evaluation phase while the PDN is active, using the LTSpice tool and 45nm PTM [20] technology.

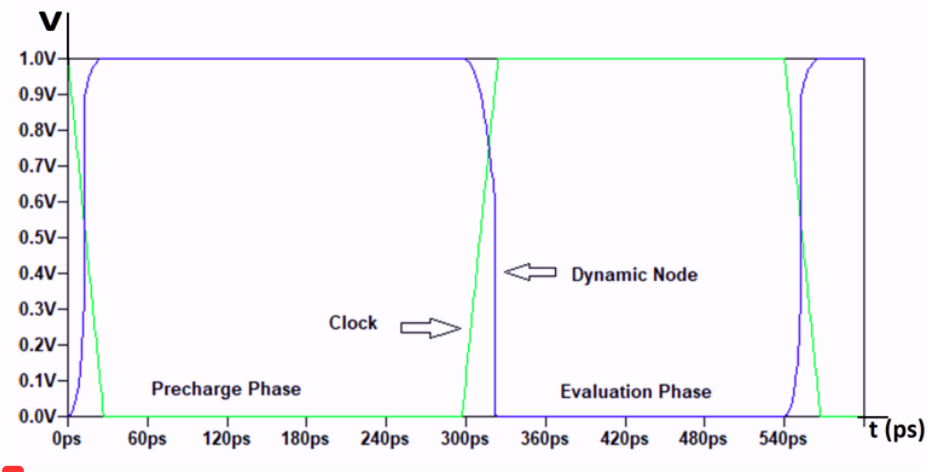

Fig. 4.1 Simulated waveform of proposed scheme in evaluation phase when the PDN is ON with supply voltage 1V (8-bit OR logic gate)

4.2 Simulation results for wide fan-in OR logic gate operation

Table 4.1 Comparison of propagation delay between proposed model and other models for 8-bit OR logic gate with supply voltage 1V

Compared Models	Propagation Delay (ps)
Basic Domino	136.5
Footer Domino [3]	90
Mahbubul et al. [13]	65.5
Meher et al. [7]	55.5
Shiksha et al. [16]	76
Proposed Domino	34.72

Table 4.2 Comparison of leakage power between proposed model and other models for 8-bit OR logic gate with supply voltage 1V

Compared Models	Leakage Power (ţW)
Basic Domino	16.87
Footer Domino [3]	11.32
Islam et al. [2]	9.76
Mahbubul et al. [13]	8.59
Meher et al. [7]	6.35
Shiksha et al. [16]	5.28
Proposed Domino	4.31

In table I, the propagation delay of the proposed model has been compared with different models for the 8-bit OR logic gate operation with supply voltage 1V. In comparison to several domino logic models, the suggested model has the lowest propagation delay. In table II, comparison of leakage power between proposed model and other models for 8-bit OR logic gate with supply voltage 1V is shown. In comparison to several domino logic models, the suggested model has the lowest leakage power.

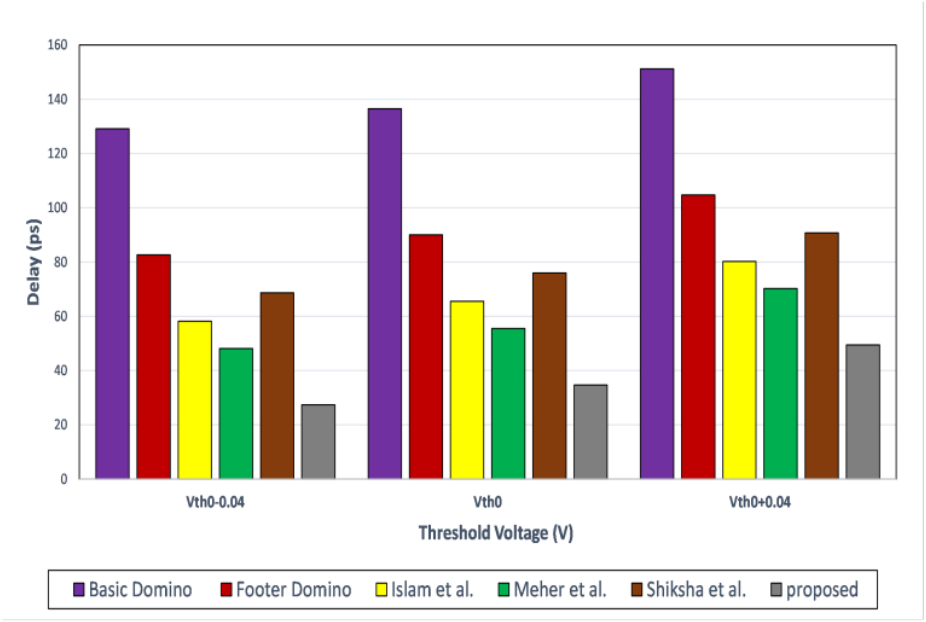

Fig. 4.2 Variation in propagation delay of the proposed model for 8-bit OR logic gate with supply voltage 1V at different threshold voltages

Fig. 4.2 shows the variation in propagation delay of the proposed model for a 8-bit OR logic gate with a supply voltage of 1V at different threshold voltages. The delay increases as the threshold voltage is increased. We have compared our proposed model with some traditional domino logic and recent domino logic. In comparison to several domino logic models, the suggested model has the lowest propagation delay.

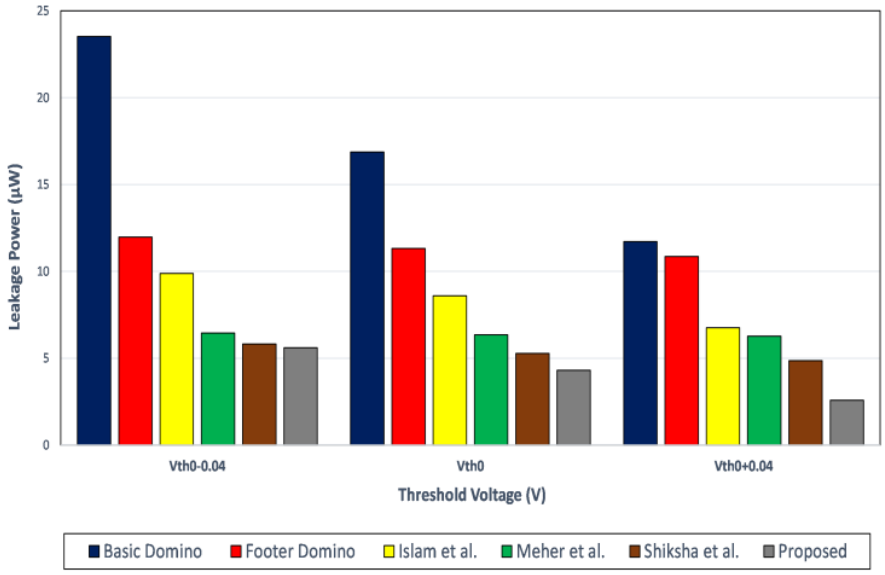

Fig. 4.3 Variation in the leakage power of the proposed model at different threshold voltages for 8-bit OR logic gate operation with supply voltage 1V

Fig. 4.3 shows the variation in leakage power of the proposed model for a 8-bit OR logic gate with a supply voltage of 1V at different threshold voltages. The leakage power decreases as the threshold voltage is increased. We have compared our proposed model with some traditional domino logic and recent domino logic. In comparison to several domino logic models, the suggested model has the lowest leakage power.

The propagation delay of the proposed model with different width to length ratio for 8-bit OR logic gate with supply voltage 1V is shown in **Fig. 4.4**. The delay here is increasing as the W/L ratio rises. Furthermore, the width to length ratio of PDN can be reduced to prevent sub-threshold leakage current.

Fig. 4.5 shows the variation in leakage power of the proposed model for various fan-in OR logic gate with varied supply voltages. The leakage power decreases as the supply voltage is decreased. We have compared between some traditional domino logic and

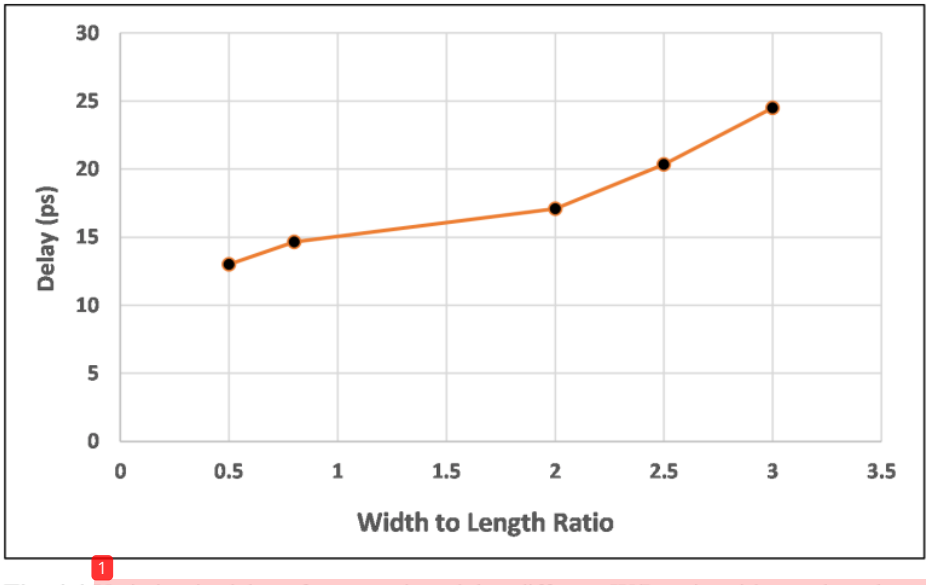

Fig. 4.4 Variation in delay of proposed model at different W/L ratio with supply voltage 1V (8-bit OR logic gate operation)

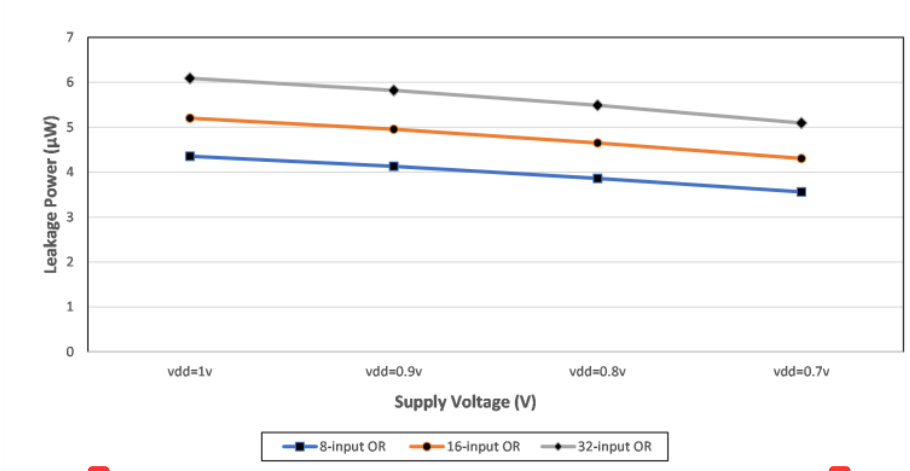

Fig. 4.5 Variation in the leakage power of the proposed model for various fan-in OR logic gate operation with different supply voltages

recent domino logic. In comparison to several domino logic models, the suggested model has the lowest leakage power.

4.3 Simulation results for wide fan-in AND logic gate operation

Fig. 4.6 shows the variation in leakage power of the proposed model for various fan-in AND logic gate with varied supply voltages. The leakage power decreases as the

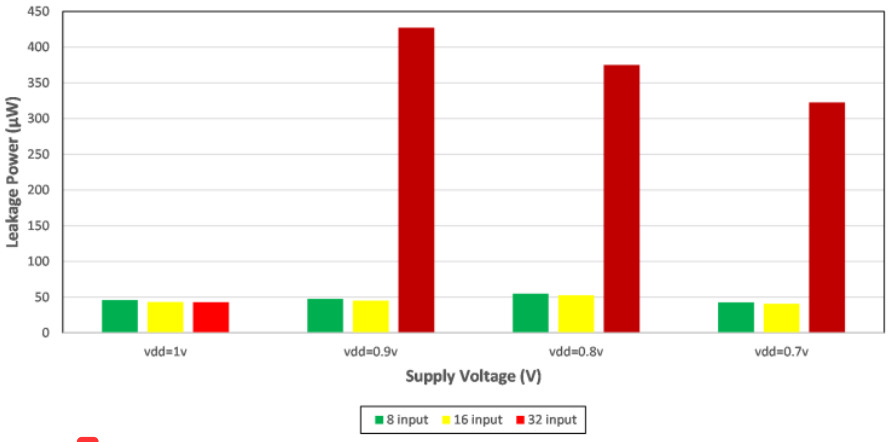

Fig. 4.6 Variation in the leakage power of the proposed model for various fan-in AND logic gate operation with different supply voltages

supply voltage is decreased. We have compared between some traditional domino logic and recent domino logic. In comparison to several domino logic models, the suggested model has the lowest leakage power.

CHAPTER 5

CONCLUSION

5.1 Introduction

Wide fan-in domino gates are more compact, resulting in more sub-threshold leakage current channels. When the PDN is OFF, noise from any source comes at gates and develops a gate to source voltage. It also causes sub-threshold leakage power causing crosstalk. So, reducing the leakage power is a great challenge while designing a dynamic logic circuit. A new design technique for the dynamic logic circuit is described in this thesis, which significantly minimizes the leakage power and propagation delay. By adding delay components and adjusting the stacking effect circuitry below the PDN, the leakage power and delay is decreased. It may be made even better by scaling the size of the transistors utilized in the proposed model. The OR-AND logic gate operation is taken into account in the PDN. An alternative version of the suggested model may be built using any complex logic gate operation. On LTSpice, the proposed model is simulated using 45nm PTM technology. The proposed model outperforms mentioned models in terms of leakage power reduction of at least 18% and propagation delay reduction of at least 37% for wide fan-in gates. As a result, the proposed model is suitable for both low-power and high-speed applications.

5.2 Application of this work

A new design technique for the dynamic logic circuit is described in this thesis, which significantly minimizes leakage power and propagation delay. The proposed model outperforms mentioned models in terms of leakage power reduction of at least 18% and propagation delay reduction of at least 37% for wide fan-in gates. The proposed model is suitable for both low-power and high-speed applications.

5.3 Limitation

In this thesis, leakage power and propagation delay are mainly focused on. Dynamic logic circuits have other important improvement parameters, like noise margin and overhead area. This model significantly improves leakage power and propagation delay compared to several existing models. Issues are still left as this model doesn't improve the noise margin and overhead area. Study is being continued on dynamic logic circuits so that the

mentioned parameters can be improved.

5.4 Suggestion for future work

This model may be made even better by scaling the size of the transistors utilized in the proposed model. Latest Predictive Technology Model (PTM) may be used to get better performance. These approaches may be used to calculate the relationship between static power dissipation and propagation delay and threshold voltage scaling and temperature fluctuation. For further development, this model's noise margin and overhead area determination may be done.

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APPENDIX

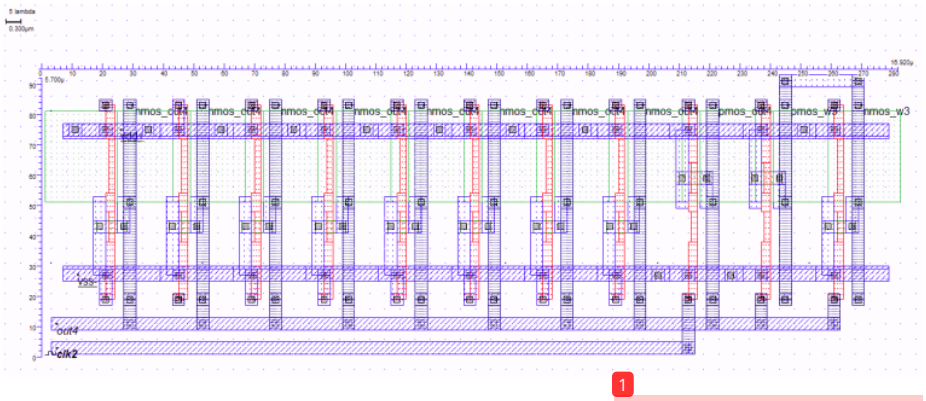

Fig. 5.1 Layout design of basic domino logic circuit for 8-bit OR logic gate with supply voltage 1V

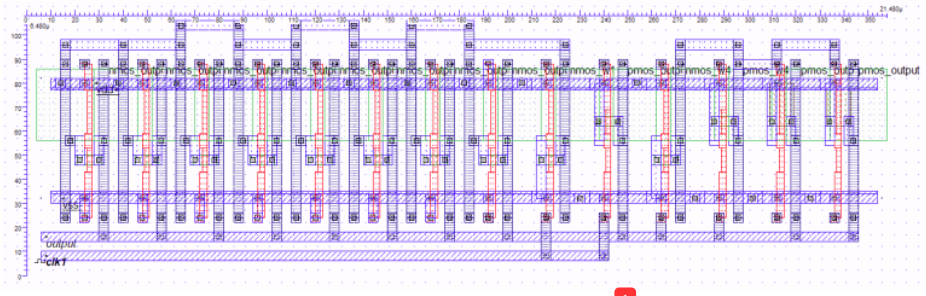

Fig. 5.2 Layout design of footer domino logic circuit for 8-bit OR logic gate with supply voltage 1V

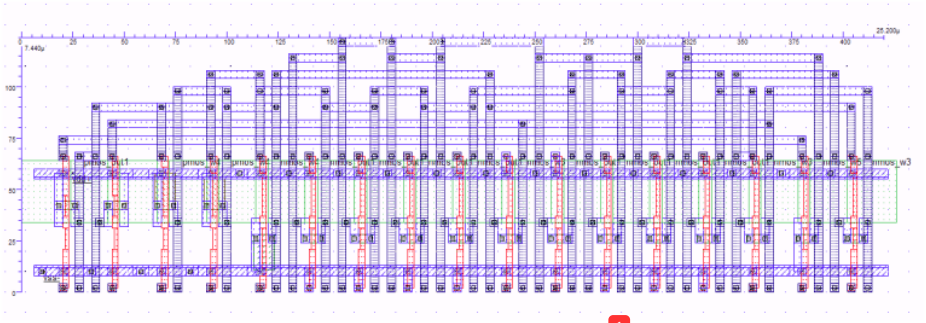

Fig. 5.3 Layout design of Islam et al. domino logic for 8-bit OR logic gate with supply voltage 1V

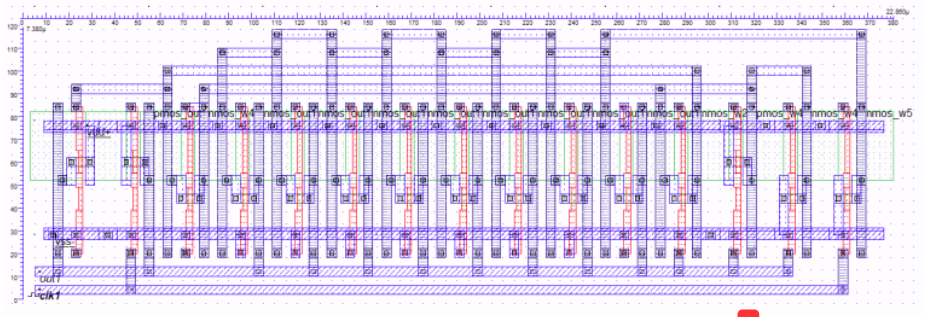

Fig. 5.4 Layout design of mahbubul et al. domino logic circuit for 8-bit OR logic gate with supply voltage 1V

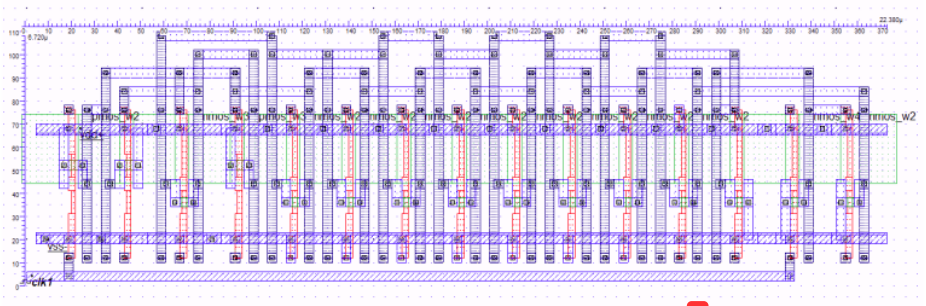

Fig. 5.5 Layout design of Meher et al. domino logic circuit for 8-bit OR logic gate with supply voltage 1V

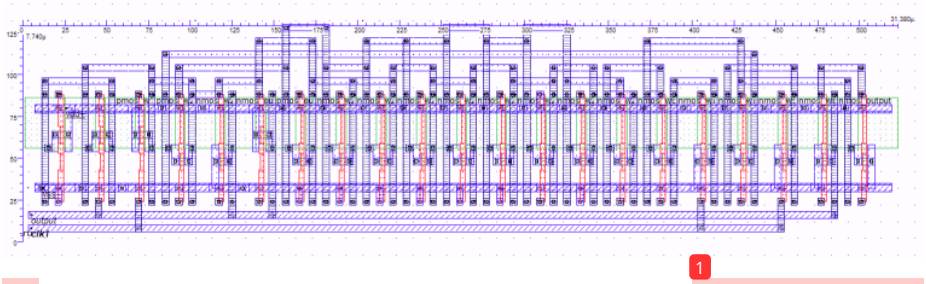

Fig. 5.6 Layout design of shiksha et al. domino logic circuit for 8-bit OR logic gate with supply voltage 1V

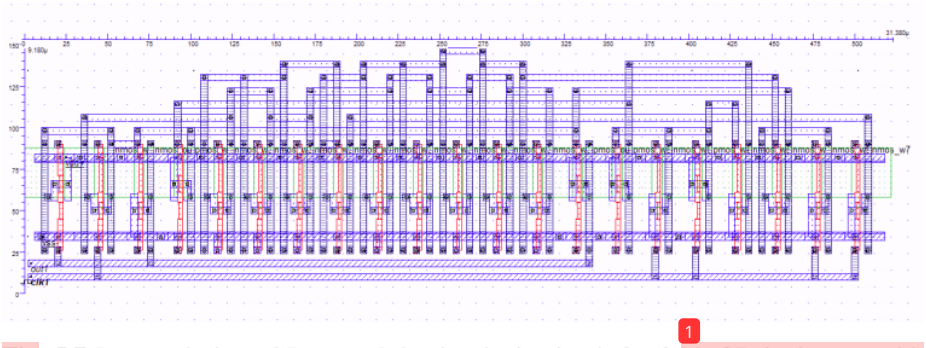

Fig. 5.7 Layout design of Proposed domino logic circuit for 8-bit OR logic gate with supply voltage 1V

Table 5.1 Comparison of propagation delay between proposed model and other models for 8-bit OR logic gate with supply voltage 1V when Vth=Vth0-0.04

Compared Models	Propagation Delay (ps)
Basic Domino	129.14
Footer Domino	82.64
Mahbubul et al.	58.14
Meher et al.	48.14
Shiksha et al.	68.64
Proposed Domino	27.36

Table 5.2 Comparison of propagation delay between proposed model and other models for 8-bit OR logic gate with supply voltage 1V when Vth =Vth0+0.04

Compared Models	Propagation Delay (ps)
Basic Domino	151.22
Footer Domino	104.72
Mahbubul et al.	80.22
Meher et al.	70.22
Shiksha et al.	90.72
Proposed Domino	49.44

Table 5.3 Comparison of leakage power between proposed model and other models for 8-bit OR logic gate with supply voltage 1V when Vth= Vth0-0.04

Compared Models	Leakage Power (ţW)
Basic Domino	23.52
Footer Domino	11.97
Islam et al.	8.69
Mahbubul et al.	9.88
Meher et al.	6.45
Shiksha et al.	5.82
Proposed Domino	5.6

Table 5.4 Comparison of leakage power between proposed model and other models for 8-bit OR logic gate with supply voltage 1V when Vth = Vth0+0.04

Compared Models	Leakage Power (ţW)
Basic Domino	11.72
Footer Domino	10.86
Islam et al.	9.74
Mahbubul et al.	6.75
Meher et al.	6.27
Shiksha et al.	4.86
Proposed Domino	2.58

Table 5.5 Leakage power of proposed model for 16-bit OR logic gate with different threshold voltages with supply voltage 1V

Compared Models	Leakage Power (ţW)
Basic Domino	23.735
Footer Domino	15.712
Mahbubul et al.	9.9895
Meher et al.	6.0729
Shiksha et al.	7.9308
Proposed Domino	5.2

Table 5.6 Leakage power of proposed model for 16-bit OR logic gate with Vth=Vth0-0.04 for supply voltage 1V

Compared Models	Leakage Power (ţW)
Basic Domino	30.034
Footer Domino	16.415
Mahbubul et al.	11.409
Meher et al.	6.2478
Shiksha et al.	7.9439
Proposed Domino	7.64

Table 5.7 Leakage power of proposed model for 16-bit OR logic gate with Vth=Vth0+0.04 for supply voltage 1V

Compared Models	Leakage Power (ţW)
Basic Domino	16.962
Footer Domino	15.053
Mahbubul et al.	7.3857
Meher et al.	6.0093
Shiksha et al.	6.8953
Proposed Domino	3.23

Table 5.8 Leakage power of proposed model for 16-bit OR logic gate with different supply voltages

Supply Voltage (Vdd)	Leakage Power (ţW)
1V	5.2008
0.9V	4.9542
0.8V	4.652
0.7V	4.3068

Table 5.9 Leakage power of proposed model for 32-bit OR logic gate with different threshold voltages at supply voltage 1V

Threshold Voltage (V)	Leakage Power (ţW)
Vth0	6.09
Vth0-0.04	8.72
Vth0+0.04	3.91

Table 5.10 Leakage power of proposed model for 8-bit OR logic gate with different supply voltages

Supply Voltage (Vdd)	Leakage Power (ţW)
1V	4.3555
0.9V	3.7185
0.8V	3.0893
0.7V	2.4936

Table 5.11 Leakage power of proposed model for 32-bit OR logic gate with different supply voltages

Supply Voltage (Vdd)	Leakage Power (ţW)
1V	6.0898
0.9V	5.2391
0.8V	4.3909
0.7V	3.5651

Table 5.12 Leakage power of proposed model for 8-bit AND logic gate with different threshold voltages at supply voltage 1V

Threshold Voltage (V)	Leakage Power (pW)
Vth0	45.967
Vth0-0.04	57.814
Vth0+0.04	506.6

Table 5.13 Leakage power of proposed model for 8-bit AND logic gate with different supply voltages

Supply Voltage (Vdd)	Leakage Power (pW)
1V	45.967
0.9V	52.854
0.8V	68.602
0.7V	61.213

Table 5.14 Leakage power of proposed model for 16-bit AND logic gate with different threshold voltages at supply voltage 1V

Threshold Voltage (V)	Leakage Power (pW)
Vth0	43.398
Vth0-0.04	51.864
Vth0+0.04	504.83

Table 5.15 Leakage power of proposed model for 16-bit AND logic gate with different supply voltages

Supply Voltage (Vdd)	Leakage Power (pW)
1V	43.398
0.9V	45.252
0.8V	52.836
0.7V	40.8653

Table 5.16 Leakage power of proposed model for 32-bit AND logic gate with different supply voltages

Supply Voltage (Vdd)	Leakage Power (pW)
1V	43.025
0.9V	427.356
0.8V	375.04
0.7V	322.651

Table 5.17 Leakage power of proposed model for 32-bit AND logic gate with different threshold voltages at supply voltage 1V

Threshold Voltage (V)	Leakage Power (pW)
Vth0	43.025
Vth0-0.04	49.882
Vth0+0.04	504.77

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