International Islamic University Chittagong (IIUC)

Department of Electronic and Telecommunication Engineering

Final Examination

Program: B.Sc (Engg.) | **Semester: Spring'2023**

Course Code: ETE-4827/4847 | **Course Title: VLSI System Design & Modeling**

Total Marks: 50 | **Time: 2.5Hours**

[(i) Answer all the questions. The figures in the right-hand margin indicate full marks.]

[(ii) Course Learning Outcomes (COs) and Bloom's Levels are mentioned in additional Columns.]

Course Outcomes (COs) of the Questions	
CLO1	Identify and understanding the basic knowledge of VLSI technology and Circuit.
CLO2	Recognize and illustrate the theoretical knowledge of MOS circuit device design and fabrication.
CLO3	Apply and Analyze the knowledge to design different sequential and combinational login circuit using NMOS, PMOS and CMOS.

Bloom's Levels of the Questions						
Letter Symbols	**R**	**U**	**Ap**	**An**	**E**	**C**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

Group A

Q1.	(a)	Describe the step by step p-MOS fabrication process with diagram.	05	CLO2	An
	(b)	Describe the step by step p-well CMOS fabrication process with necessary diagram.	05	CLO2	U, An
		OR			
Q2.	(a)	Distinguish between Electron beam lithography and Ion beam lithography system.	05	CLO2	An
	(b)	Distinguish between pin-through-hole and surface –mount-technology package of VLSI system.	05	CLO2	An
Q3.	(a)	Design a layout diagram for the Boolean function $Y = (AC + BD)(CB + AD)$ and sketch the stick diagram using CMOS.	10	CLO3	C

Group B

Q4.		Design a CMOS 3 bit even and odd parity generator and sketch the stick diagram.	10	CLO3	C
		OR			
Q5.		Design a CMOS 3 bit even and odd parity checker and sketch the stick diagram.	10	CLO3	C
Q6.	(a)	Discuss the Gate array design of chip implementation design style.	05	CLO2	An
	(b)	Discuss the Full custom Design for CMOS implementation.	05	CLO2	An
Q7.	(a)	Write the VHDL application field and benefits.	05	CLO2	U
	(b)	Write a program for 2 bit adder circuit using Verilog HDL code.	05	CLO3	C