

INVERTER BASED DISTRIBUTED GENERATION PROTECTION SCHEME USING BRIDGE TYPE FAULT CURRENT LIMITER

by

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ENGINEERING**



Department of Electrical and Electronic Engineering
INTERNATIONAL ISLAMIC UNIVERSITY CHITTAGONG

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CERTIFICATE OF APPROVAL

The thesis entitled as **“Inverter based distributed generation protection scheme using bridge type fault current limiter”** submitted by **Muhammad Azharul Islam**, bearing Matric ID. **ET-161012** and **Ashrafur Rahman**, bearing Matric ID. **ET-161037** of session **Autumn 2019**, to the Department of Electrical and Electronic Engineering, International Islamic University Chittagong, has been accepted as satisfactory in partial fulfilment of the requirements for the degree of Bachelor of Science in Engineering and approved for the examination held on **28 July, 2020**.



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DECLARATION

It is hereby declared that this work has been done by us and no portion of the work contained in this thesis has been submitted elsewhere for the award of any degree or diploma.

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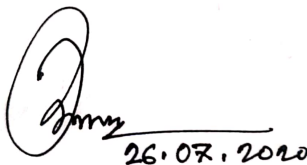
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Muhammad Azharul Islam



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ABSTRACT

Power systems are becoming more vulnerable to different faults due to high penetration of various renewable energy based distributed generators known as inverter based distributed generator (IBDG). It has become a great challenge to keep the system stable and to keep the fault current at a manageable range during a short circuit fault. High fault current insists system designer to install high rated protection equipments which increases the overall cost of the system. While connecting an IBDG system to the grid, it's protection scheme must be considered because of this fault current problem. In this work, a bridge type fault current limiter (BFCL) with a proper control of the whole system has been proposed as a solution to the high fault current problems of IBDG systems. The BFCL is connected to the AC side of IBDG system and a proper controller is designed and implemented to control the reactance of BFCL. Voltage at point of common coupling (PCC) is used as input to the BFCL activation controller. Outer controller loop is proposed to control the DC link voltage of IBDG whereas an inner current controller is designed to control the power exchange between AC and DC side of IBDG. Both the balanced and unbalanced faults are applied in the AC side of the IBDG system to demonstrate the effectiveness of the proposed controller. Finally the proposed strategy is compared with series dynamic braking resistor (SDBR) and conventional method to see the effectiveness of the proposed strategy.

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LIST OF ABBREVIATIONS

IBDG	Inverter Based Distributed Generation
SHS	Solar Home System
BFCL	Bridge Type Fault Current Limiter
SDBR	Series Dynamic Braking Resistor
SC	Short Circuit
CB	Circuit Breaker
TFCL	Tolerable Fault Current Limit
CLF	Current Limiting Fuse
CLCB	Current limiting Circuit Breaker
FCL	Fault Current Limiter
SFCL	Superconducting Fault Current Limiter
HTS	High Temperature Superconductor
SSFCL	Solid State Fault Current Limiter
RSFCL	Resistive Type Superconducting Fault Current Limiter
ISFCL	Inductive Type Superconducting Fault Current Limiter
BHFCL	Bridge Type Hybrid Fault Current Limiter
MBFCL	Modified Bridge Type Fault Current Limiter
VSC	Voltage Source Converter
FRT	Fault Ride Through
LVRT	Low Voltage Ride Through

CHAPTER 1

INTRODUCTION, BACKGROUND

1.1 Introduction

Since the dawn of industrialization, world energy demand is increasing very rapidly. To fulfil the high demand of energy, the power sector has also expanded almost at the same rate. Fossil fuels are the major sources of raw materials for power generation since then. Coal and oil based power plants were the primary sources of electricity up to the mid of 20th century, later natural gas and nuclear energy based power plants share a portion of coal and oil. Continuous usage of fossil fuels over the centuries for energy production has risen some key issues like huge greenhouse gas emission, extensive environment pollution, ecological imbalance. As a consequence of these, humankind are going to face some irrecoverable environmental problems like global warming, damaging of ozone layer, arctic ice melt, rise of sea level and flooding of vast living areas [1]–[4]. Because of all these major issues of burning fossil fuels and the rise of environmental concerns, researchers started to seek for alternative to fossil fuels since the mid of 20th century. A number of solution has been found: solar pv cell, wind energy, biomass and biofuels are the most used alternatives of fossil fuels widely known as renewable energy sources [5]–[8]. Renewable energy sources have the ability to reduce the effect of these issues caused by fossil fuels at a good extent. Renewable energy sources have some direct advantages over fossil fuels such as significantly less greenhouse gases especially CO_2 emission, production of overall less pollutant, more eco-friendly and theoretically infinite storage of fuels [9], [10]. Because of these advantages integration of renewable energy based power generation system into the existing power system is increasing every year. The share of all renewable energy sources in Q1 2020 is about 28% which was 26% in Q1 2019 [11].

Renewable energy sources based on solar pv and wind turbine needs inverter to get connected with the grid and such generation system is known as inverter based distributed generation (IBDG). Large amount of integration of IBDG system solves many problems of conventional power generation system also creates some new challenges for the protection, stability, dynamic performances of the power system [12], [13]. In renewable energy based power generation most of the sources are small scale and micro grid ex-

cept some solar stations ranging from several hundred MW to 1.5 GW. The addition of many generators in the distribution network is problematic, since it causes high bi-directional fault currents and sympathetic tripping [14], [15]. Another major problem of having many generation systems in a power system is the dramatic increase of short circuit (SC) fault current level because of the parallel connection of the inverter based distributed generation with the grid which results in low source impedance of the generation station [16]. Because of this two major reasons IBDG systems are vulnerable to SC faults [17]. “**Fig. 1.1**” shows block diagram of a fault affected grid connected IBDG system.

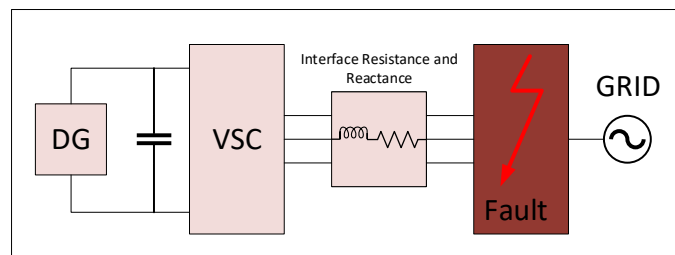


Figure 1.1 Fault in IBDG system

In this work, we have proposed a solid state fault current limiter (SSFCL) known as bridge type fault current limiter (BFCL) for the protection of IBDG system against AC/DC faults. A controller has been designed for the inverter based distributed generation system. Both symmetrical and unsymmetrical faults are applied to see the effectiveness of the proposed methodology. Simulations have been done using MATLAB/Simulink. “**Fig. 1.2**” shows a simple block diagram of our proposed system to limit the fault current in inverter based distributed generation system.

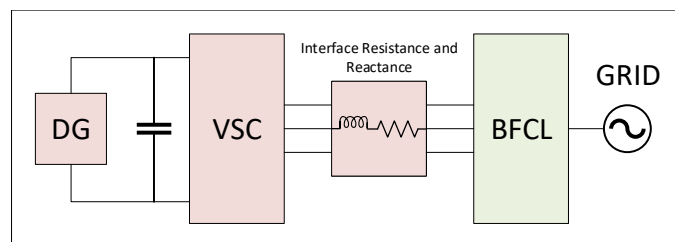


Figure 1.2 Proposed IBDG system

1.2 Objectives of this work

1. Providing a background of power system faults, effects of faults and protection measures against fault current.
2. Modeling of IBDG system

3. Designing of a controller for the IBDG system for the efficient operation and DC to AC conversion for grid connection
4. Designing a BFCL based protection framework for the IBDG system to limit fault current
5. Simulation of the IBDG system with the proposed protection framework and comparing the results with SDBR based protection framework.

1.3 Fault current in power system

Fault is an unwanted, unpredictable and abnormal condition which tends to create failure in the normal operation of power system and causes damage to the equipments. Two types of failure are seen in a power system when a fault occurs

1. Insulation failure which causes SC fault
2. Stoppage of current flow which causes open circuit fault

Most of the faults are SC faults. During a SC fault, the current flow of the circuit can increase up to 10 times of steady state current flow of the circuit depending on the severity of the fault. This excessive over flow of current at the time of a fault is known as 'fault current'. As the fault current level rises, the protective devices rating also increases which rise the cost of the overall system [18].

1.3.1 Types of power system fault

There are two main types of fault seen in power system. Symmetrical or balanced faults and unsymmetrical or unbalanced faults. Two types of symmetrical faults are seen in power system, first one is 3 phase short circuit fault and second one is 3 phase to ground fault. There are three types of unsymmetrical faults: 2 phase to ground fault, single phase to ground fault, 2 phase SC fault [18]. None of the symmetrical faults make any disturbances in the phase sequence and their angles, symmetry of balance doesn't get hampered for which they are called symmetrical or balanced faults. In terms of fault current magnitude symmetrical faults are the deadliest. It has been seen that 3 phase to ground fault creates the highest magnitude of fault current among all symmetrical and unsymmetrical faults. Block diagram of symmetrical faults is shown in "**Fig. 1.3**". The symmetry of the phase sequence and phase angles breaks down in unsymmetrical faults. Block diagram of unsymmetrical faults is shown in "**Fig. 1.4**".

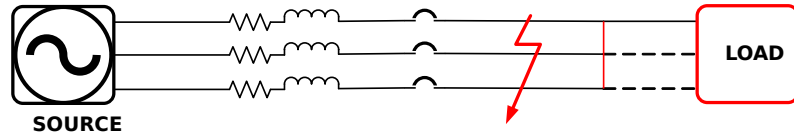


Fig. 1.3.a 3 phase short circuit fault

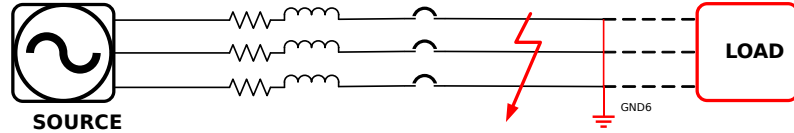


Fig. 1.3.b 3 phase to ground fault

Figure 1.3 Symmetrical faults

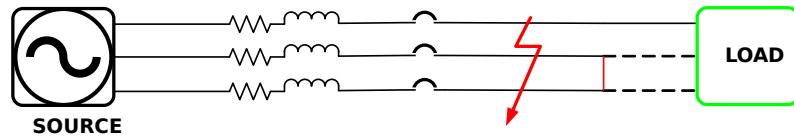


Fig. 1.4.a 2 phase short circuit fault

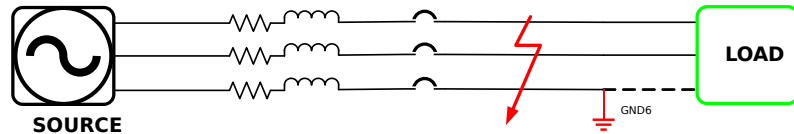


Fig. 1.4.b Single phase to ground fault

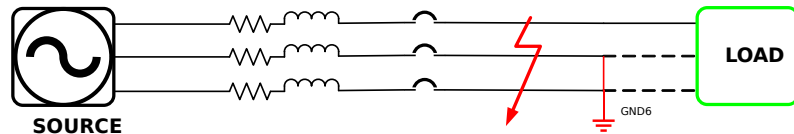


Fig. 1.4.c 2 phase to ground fault

Figure 1.4 Unsymmetrical faults

1.3.2 Impacts of fault on power system as a whole

The impacts of SC fault on a power system depends on many variables such as: number of generation station, types of generation station, types of load, protection system, condition of the equipments and many more. Although the impacts of a fault largely depends on these variables but a fault always creates disturbances in the normal operation of the system. The common impacts of fault is given below [19].

- Power interruption
- Damped mechanical oscillations on the generators and motors' shaft
- Negative rotational inertia and stress on the damping windings of synchronous machines
- Increase in the reactive power demanded by inductive impedance of the transmission lines and leakage impedance of power transformers

- Voltage drop in buses with voltage-sensitive loads
- Torque reduction in induction motors
- Thermal stress on equipment
- Voltage swell and voltage sag in un-faulted buses
- Electromagnetic interference
- Increased unsupplied energy and economic losses
- Corrosion in the connection area
- Reduction in power system reliability and power quality indexes

To visualize the impacts of faults on a power system, both symmetrical and unsymmetrical faults are applied in the following system of “**Fig. 1.5**”. The simulation has been run for 0.2 second. The fault is applied from 3rd to 6th cycle and both circuit breaker are tripped at 8th cycle so that the fault condition can be visualised.

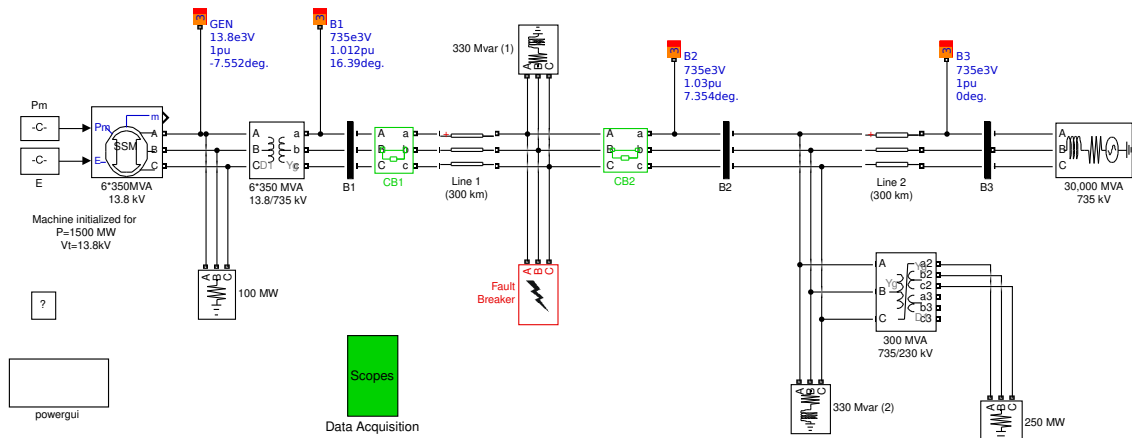


Figure 1.5 Example power system

Voltage and current measurement are taken at B_1 and B_2 places of the transmission system. Measurements are done in per unit (PU).

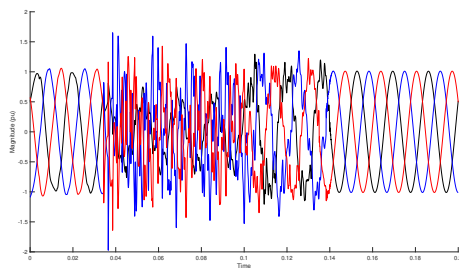


Fig. 1.6.a Voltage at B_1

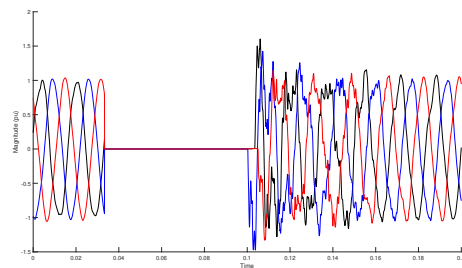


Fig. 1.6.b Voltage at B_2

Figure 1.6 System voltage during a 3 line to ground fault

The impact of a 3lg fault on the voltage is depicted in “**Fig. 1.6**”. We see that at B_1 , the phase disturbance is very high during the fault, the system recovers it’s steady state condition after terminating the connection with the faulty section at 8th cycle. At B_1 , there is no voltage during the fault because the 3lg fault occurred between the this section and the generating station. Voltage condition during a 2lg fault is shown in “**Fig. 1.7**”.

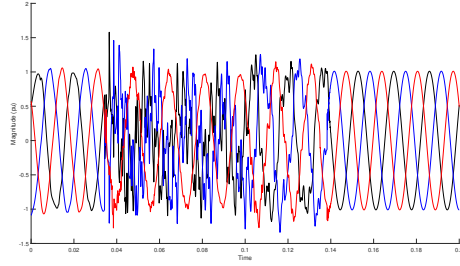


Fig. 1.7.a Voltage at B_1

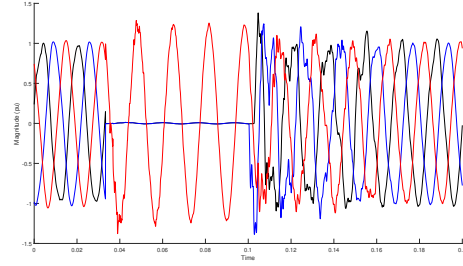


Fig. 1.7.b Voltage at B_2

Figure 1.7 System voltage during a 2 line to ground fault

System current during a 3lg and 2lg faults are shown in “**Fig. 1.8**” and “**Fig. 1.9**” respectively.

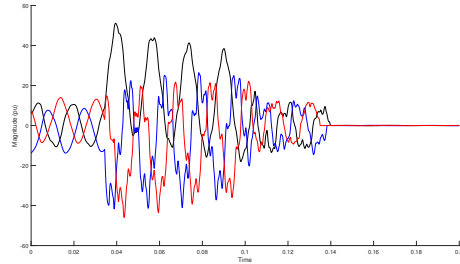


Fig. 1.8.a Current at B_1

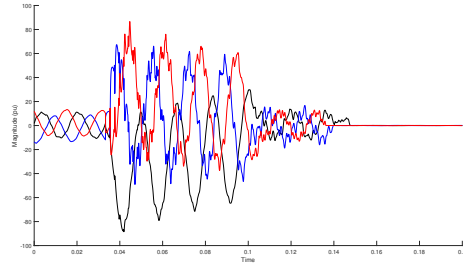


Fig. 1.8.b Current at B_2

Figure 1.8 System current during a 3 line to ground fault

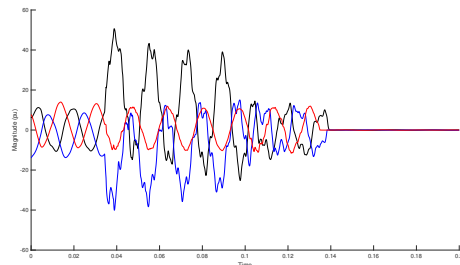


Fig. 1.9.a Current at B_1

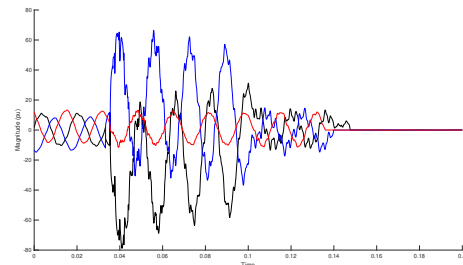


Fig. 1.9.b Current at B_2

Figure 1.9 System current during a 2 line to ground fault

1.4 Protection measures against fault current

“Fig. 1.10” illustrates some of the most common approaches of fault current limitation. There are two main approaches for limiting fault current, topology and apparatus based approaches. Apparatus based approaches use physical devices for limiting fault current. There are two principles of limiting fault current, passive and active principles. In passive principles, high impedance is added to the system to limit fault current both at normal and fault condition. Hence voltage drop is obvious at operation condition of the system which decreases the system efficiency significantly. On the other hand active principles add impedance to the system to limit the fault current only at fault condition.

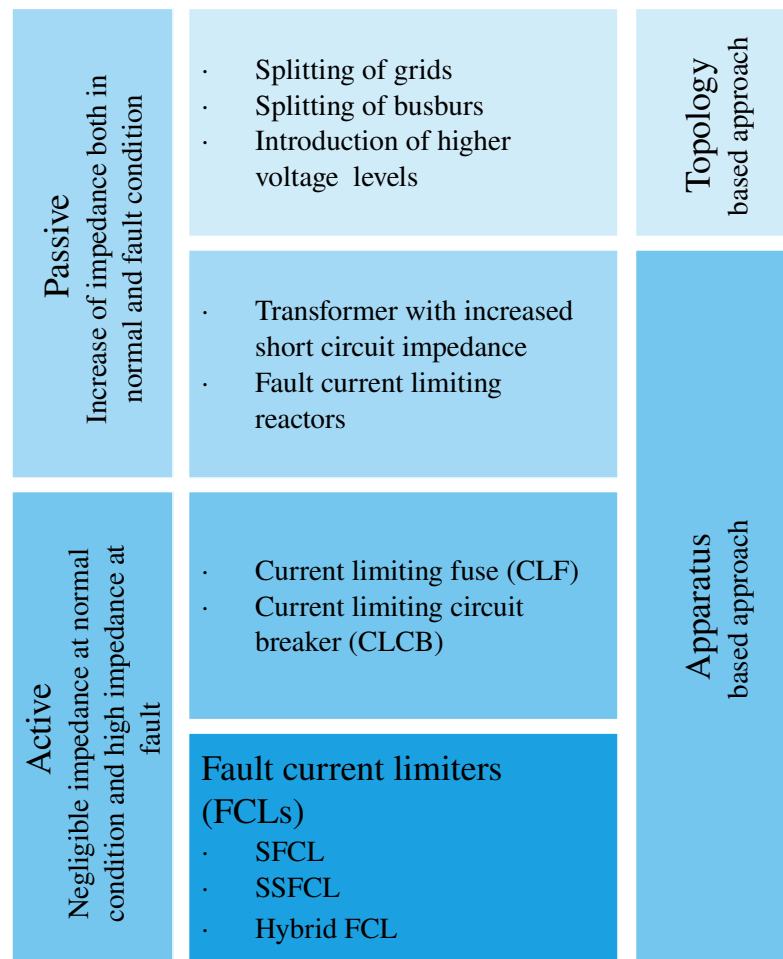


Figure 1.10 Approaches towards fault current protection [20]

To ensure power system protection against fault current circuit breakers, current limiting reactor, fuses and sectionalizers [21]–[23] are being used for a long time. Current limiting fuse (CLF) and current limiting circuit breaker (CLCB) are widely used for limiting excessive fault current as a primary solution. CLFs and CLCBs are being used in power system since 1930. CLFs and CLCBs terminate the connection between faulty section

and the rest during a fault. Thus the system is protected from excessive fault current.

However all of these protection devices have some drawbacks. Current limiting reactors insert impedance in the normal operation of the system. CLFs needs to replace after each operation and can't operate at high voltage level [24]. Circuit breakers usually operate after the first few cycles (1 or 2) of the fault current to interrupt the fault and it's effect. But the first cycle of fault current has the highest magnitude and may cause serious damage to the system [25]. Moreover circuit breakers and fuses have a particular tolerable fault current limit (TFCL), up to the TFCL limit these protective devices works perfectly. So for protection against high fault current, devices with high TFCL are necessary. For example, to design a protection scheme for the system of “**Fig. 1.5**”, the circuit breakers, current transformers (CTs), Power transformers (PTs) and other peripheral devices rating must be at least 4 to 6 times of the steady state current of the system because the current is rising up to 4 to 6 times of the steady state current of the system as shown in “**Fig. 1.8**” and “**Fig. 1.9**”. Such high ratings of protection and measurement devices increases the cost of the system dramatically. So, the main goal is to limit this very high rating of SC current at a tolerable range . All of these problems of these fault current limiting devices encouraged researchers to find out for a better fault current limiting solution.

Fault current limiter (FCL) technologies are considered as a better solution towards these problems. FCLs are now widely used for limiting fault current with minimal power interruption . CLFs and CLCBs break the connection between faulty and un-faulty section while FCLs insert a high impedance in the system to limit the excessive fault current as soon as a fault occur. But for the normal operation this high impedance is kept at a negligible range by using some mechanism. Based on these mechanisms and technologies FCLs are classified into different groups. A details discussion on fault current limiters is presented on chapter 2. By using fault current limiter below mentioned improvement can be achieved from a power system [19].

- Power system equipments such as circuit breakers, CTs, PTs and measurement devices need less SC rating since fault current limiter limits the SC current at a tolerable range
- After a fault operation the equipments of the system do not need to be changed.
- During the normal operation FCLs acts like a normal transmission wire. They don't

add any significant disturbances, voltage drop and impedance to the system.

- Overall system cost is lowered.
- Less power interruption during faults.
- Overall stability of the system can be improved.
- Multiple faults can be handled well with fault current limiters.

Rest of the thesis paper has been arranged in the following order. $\Rightarrow$ Chapter 2 presents literature review of this work $\Rightarrow$ chapter 3 presents the design and control mechanism of bridge type fault current limiter $\Rightarrow$ chapter 4 presents the details procedure of the system design and control design $\Rightarrow$ chapter 5 present a very detailed description of simulation of the system in MATLAB/Simulink as well as the response of the controller and different parts of the system during the simulation $\Rightarrow$ the outcomes of this work is presented in chapter 6 and chapter 7 concludes this thesis paper.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview of fault current limiter technologies

Fault current limiters can be classified into three main groups as per the available technologies. Superconducting fault current limiter (SFCL), Solid state fault current limiter (SSFCL) and Hybrid fault current limiter.

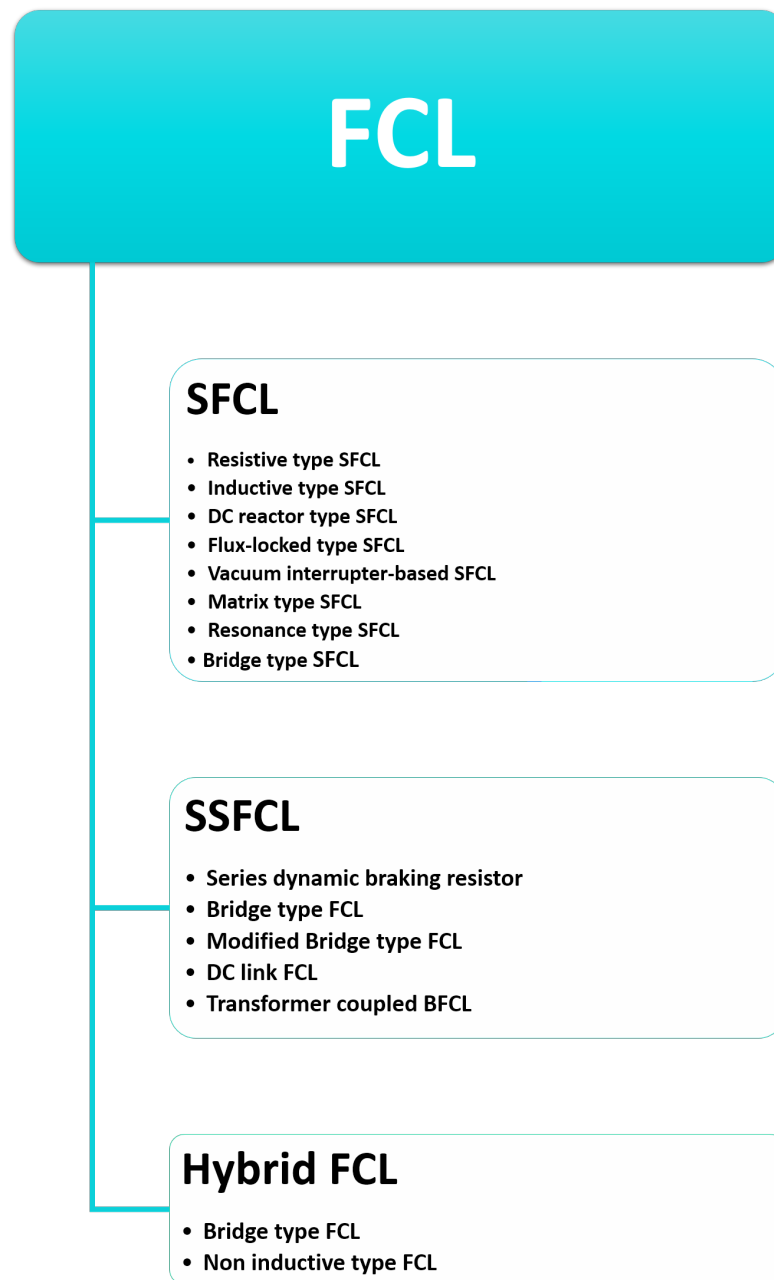


Figure 2.1 Types of fault current limiter

Each group can be further classified into various types. Some of the most commonly used

SFCLs are classified in “**Fig. 2.1**” but they are not limited to these only [19]. Among all types of FCLs, SFCLs are mostly used in power sector because of its automatic operation, high fault current limiting capability and low failure rate. But most cases choice of a FCL depends on the application.

2.1.1 Superconducting fault current limiter (SFCL)

Discovery of high temperature superconductivity (HTS) in 1986 [26] opened the horizon of applications of superconductor because of its high operating temperature. Improvement of HTS materials over the last few decades increases the operating temperature of superconductor around 70 k which is near absolute zero temperature for conventional superconductor. This high operating temperature makes it possible to use them in real time application because of the reduction of refrigeration cost up to 20 times of conventional superconductor. Although some superconductors work at much higher temperature, for example *lanthanum hydride* shows superconductivity at 250k under high pressure [27] at lab but they are not applicable for real time application.

Superconducting fault current limiter uses a superconducting coil which acts like a normal wire with almost no resistance during normal operation and acts like an insulator during a fault. The basic principle of operation is same for all superconducting fault current limiters. There are three main parameters that drives the superconductor to change its resistance: temperature, current density and magnetic field. For the normal condition, current pass through the superconductor and it doesn't resist the current because of its superconducting (zero resistance state) nature until current exceeds a certain limit. During a fault, SC current increases which increases the temperature, current density and magnetic field. So the superconductor goes to its resistive state and acts like a resistor [28], [29].

2.1.1.1 Resistive type superconducting fault current limiter (RSFCL)

The basic structure of a resistive type SFCL is shown in “**Fig. 2.2**” in its simplest form. Resistive type SFCLs are the most commonly used SFCL because of their low price compared to other SFCLs and simple operation mechanism [30]. It is called resistive SFCL because of the resistive characteristics of the superconductor. RSFCL operates based on the transition of superconductor from superconducting state to the normal conducting state known as *quench*. There is almost no resistance at the time of the normal operation of the system and the resistance starts to increase very rapidly as soon as the sc current

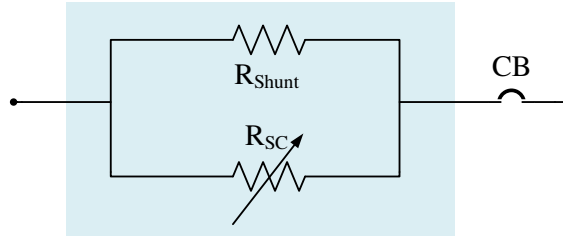


Figure 2.2 Schematic representation of RSFCL [30]

cross the current limit known as critical current of the superconductor at the time of fault. Shunt resistance (R_{shunt}) is necessary to give protection to the superconductor from destructive hotspots during the fault condition. The shunt resistance has to be connected across the length of the superconductor. The function of R_{shunt} is to adjust the limited current and avoid over-voltage that rises when R_{sc} rises rapidly [31]. Current path of RSFCL is shown in “**Fig. 2.3**”.

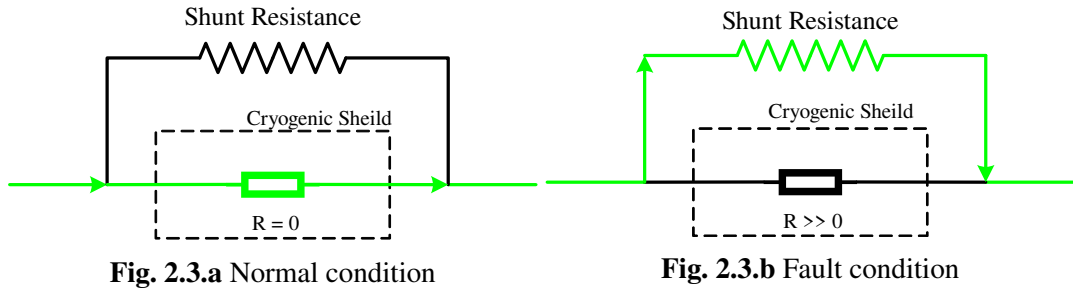


Figure 2.3 Current flow in RSFCL

2.1.1.2 Inductive type superconducting fault current limiter (ISFCL)

ISFCL uses a special type of transformer whose primary coil is made of copper (Cu) winding and secondary coil with HTS material as shown in “**Fig. 2.4**”. The primary copper (Cu) winding is connected to the system circuitry and the secondary winding which is the HTS material is kept under refrigeration in a cryostat. The HTS material can be created with superconducting tapes or bulk material like tubes [32]. ISFCLs can be configured with different configurations such as transformer type ISFCL, magnetic shield type ISFCL, rod type ISFCL. In steady state condition, superconductor in the secondary winding prevents the penetration of magnetic flux which keeps the impedance as low as possible. During the fault condition, SC current cross the critical current limit of the superconductor and it goes into resistive state. The resistance of the HTS material is reflected in the primary and the whole circuit which limits the SC fault current. The structure of a magnetic shield type ISFCL is shown in “**Fig. 2.5**”. The position of the

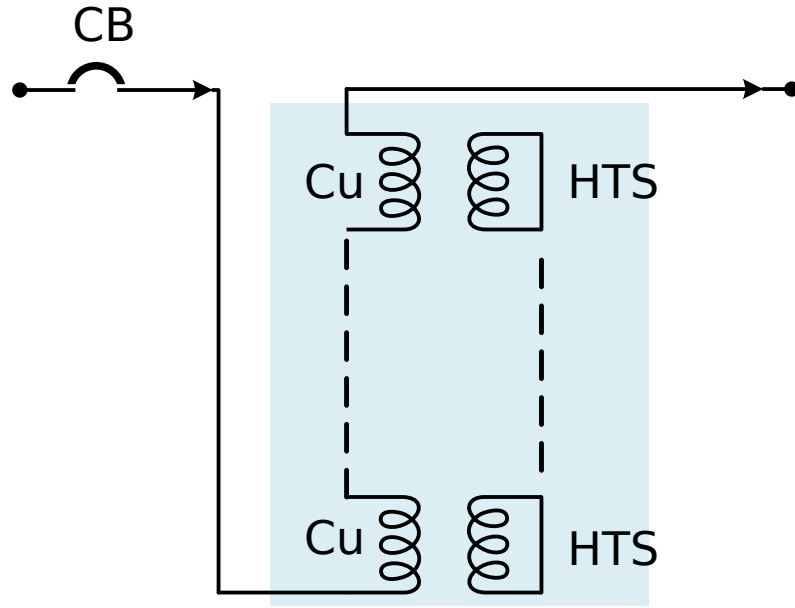


Figure 2.4 Schematic diagram of ISFCL [32]

superconducting tube is between the copper coil and the core. During the normal operation of the system no penetration of magnetic flux occurs between the core and copper coil. The core is open ended which has advantages as well as disadvantages compared to RSFCL. The advantages are low volume, low weight and low cost. The disadvantages are scattering of magnetic field and may cause damage to sensitive equipments [33]. During normal operation condition, superconducting coil is in the superconducting state so very small amount of impedance is appeared in the system from the magnetic shield ISFCL. The current increases during a SC fault which makes the superconductor to go to it's resistive state. So magnetic flux produced by the copper coil penetrates the core and it

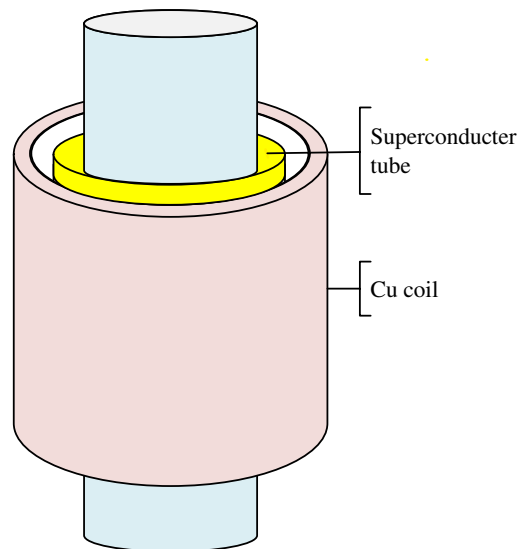


Figure 2.5 Structure of a magnetic shield type ISFCL [34]

reaches the saturation causing the impedance to increase to limit the SC fault current [35].

2.1.1.3 Flux-lock type SFCL

Flux-lock type SFCL consists of two coils and HTS material. It increases the operational current and the limiting impedance of the SFCL by making adjustment in the winding direction and the turn ratio of the coils. It also reduces the power pressure of the HTS material [36]–[38]. Schematic diagram of flux-lock type SFCL is shown in “**Fig. 2.6**”.

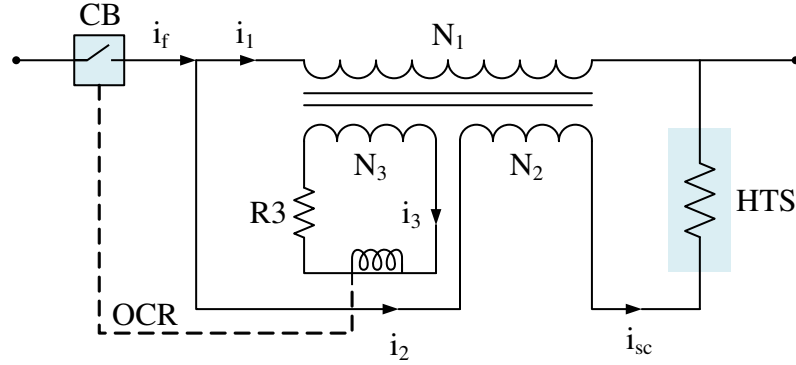


Figure 2.6 Flux-lock type SFCL [39]

Here,

$N_1 \rightarrow$ coil 1

$N_2 \rightarrow$ coil 2

$N_3 \rightarrow$ coil 3

$i_1 \rightarrow$ current in coil 1

$i_2 \rightarrow$ current in coil 2

$i_3 \rightarrow$ current in coil 3

OCR $\rightarrow$ over current relay

CB $\rightarrow$ circuit breaker

HTS $\rightarrow$ high temperature superconducting material

Flux-lock type SFCL consists of two main parts: current limiting and current interrupting parts. The current limiting part consists of two shunt connected coil and HTS element connected in series with one of the coils. Current interrupting part consists of OCR connected to one of the shunt coils and a circuit breaker.

In normal operation condition, the magnetic flux of the two coil cancels each other and doesn't induce any voltage in any coil. In fault condition, quench occurs and magnetic flux in all three coils and the SC fault current can be limited by the induced voltages in all three coils. The voltage that is induced in coil N_3 contributes to the current source to make the over current relay operational which controls the circuit breaker to perform power interruption [39].

2.1.1.4 Other SFCLs

Among all types of SFCLs resistive, inductive and resistive-inductive types are mostly implemented in real power system [19]. Resistive, inductive, flux-lock and magnetic shield type SFCLs are discussed briefly in last few sub-subsections. Since SFCLs are not the main focus of this study, so a very brief hints on other types of SFCLs are given here.

1. **DC reactor type SFCL :** A novel saturated core DC reactor type SFCL has been proposed in [40]. Based on the proposal, a 6.6 KV 100 A DC reactor type SFCL has been designed in [41].
2. **Bridge type SFCL :** It is quite hard to introduce the DC bias voltage in bridge type SFCL. A detailed analysis of this issue with varying load is presented in [42]. A bridge type SFCL without bias voltage is proposed in [43].
3. **Matrix type SFCL :** A matrix SFCL is modelled in [44]. Operational characteristics of a matrix type SFCL during ground fault is presented in [45].

A side by side comparison of above presented SFCLs are given “**Table 2.1**”.

Table 2.1 Comparison of SFCLs [46]

SFCL Types	Advantages	Disadvantages
Inductive [32], [47], [48]	• No core is necessary hence compact size and less weight	– Leakage reactance causes loss in steady state operation – To protect the superconductor from high temperature CB is obvious

Table 2.1 Continued from previous page

SFCL Types	Advantages	Disadvantages
Magnetic Shield [33], [35]	• HTS element is not directly connected to the power network, doesn't require any fault detection mechanism and more flexibility in terms of design.	– Magnetic field creates problem with sensitive devices close to it. – Unexpected voltage drop during steady state operation condition.
Resistive [30], [31], [49]	• automatically recovering characteristics, faster fault current limiting ability. • Lower cost compared to other SFCL and simple configuration.	– Long superconductor length is needed for application with high voltage – Continuous quenching can not be gained. – The dissipation of power is greater and can't recover within a short time compared to other SFCLs
Flux-lock [36]–[38]	• It increases the operational current and limiting impedance. • It also reduces the power pressure on the HTS element.	– High cost, bulk size and heavy weight.

2.1.2 Solid state fault current limiter (SSFCL)

SSFCL are favourable devices to the fault current handling application due to its inherent nature of being fast and arc-less switches [16]. SCR's, IGBT's, GTO's, ETO's, MOS-FET's and IGBT's are good switching devices which can provide almost instantly altering current path. This capability paves the way of using those devices in FCL. Multiple devices have to be stacked up in series and in parallel fashion for expanding the voltage and current rating of the package due to the limitations of the semiconductor devices in blocking voltages and current carrying [50]. However, SSFCL can play a vital role in reducing fault current and improving the dynamic stability of power systems with minimal cost compared to superconducting fault current limiters [51].

2.1.2.1 Series dynamic braking resistor (SDBR)

SDBR is a non-superconducting FCL especially used for the fault ride through capability enhancement of wind farms [52]. It is made by connecting a resistor parallelly with a switch which can be turned on and off dynamically based on the occurrence of fault in the system. The schematic diagram of SDBR is shown in “Fig. 2.7”. where IGBT

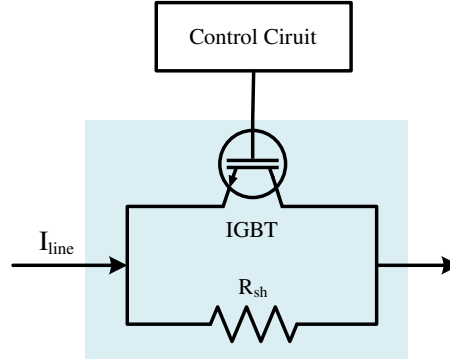


Figure 2.7 Schematic presentation of SDBR [46]

connected in series with the line is used for switching purpose due to its fast response characteristics while facing the disturbances. The control circuit generates the driving switching pulse for the IGBT. The effective value of resistance provided by SDBR is given by the following equation [53].

$$R_{SDBR} = (1 - D)R_{sh} \quad (2.1)$$

Where, R_{SDBR} is the effective resistance of SDBR, D is the duty cycle and R_{sh} is the shunt resistance.

During the normal operation, turning on of the IGBT switch bypasses the high value resistance of SDBR. In absence of any disturbances control circuits provides high voltage signal for the system and hence very small on state resistance of IGBT leads the shunt resistance being short circuited. Contrariwise, during the system disturbances variable duty cycles provided by the control circuit control the IGBT turn-on or off depending on the error of reference voltage V_{ref} and measured point of common coupling V_{pcc} . Since V_{ref} is less than V_{pcc} braking resistor continues to be in series with the line when $V_{pcc} \gg V_{ref}$ IGBT turns on and system will return to normal operation [46], [52], [53].

2.1.2.2 Modified bridge type fault current limiter (MBFCL)

The Modified Bridge type Fault current limiter(MBFCL) shown in “**Fig. 2.8**”. is the type of fault current limiters where bridge layout is rearranged to boost low voltage trip via fixed velocity capacity and variable speed wind farms [54]. The shunt direction in BFCL consists of a related resistor and inducer chain. The inductor is omitted in MBFCL, though, because it discharges When the shunt route is turned off. MBFCL bridge is

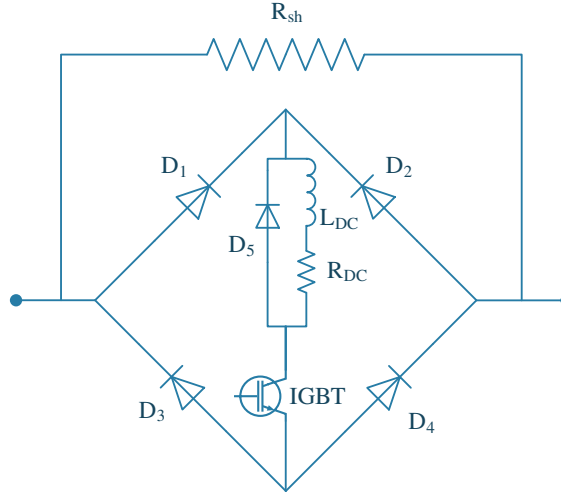


Figure 2.8 Schematic presentation of MBFCL [54]

short-circuited during normal service as the IGBT gate signal is high, thereby bypassing the branch resistance to shunting. When a malfunction pops up on the Device, the IGBT gate signal is lowered by proper control procedure, the MBFCL bridge portion is then open and shunt resistance is placed in the line to reduce the current of fault.

MBFCL have the following advantages over other other FCL technologies

- MBFCL provides a very successful way of enhancing variable speed wind turbines FRT capacity.
- Power efficiency of the network is increased and harmonic voltage coding is retained by BFCL incorporation. In addition, there is a substantial reduction in harmonic current which reduces stress on device components with an iron core, i.e. generator and transformer.
- BFCL minimizes system velocity fluctuations and improves stability.

2.1.2.3 DC link fault current limiter

To improve IBDG’s FRT functionality, it is suggested to add a DLFCL diode bridge module [55]. In “**Fig. 2.9**”, the DC link fault current limiter module is shown which is not

superconductive is Composed of a bridge diode and an inductive coil with a L_d inducer and very low resistance R_d . The DC reactor has a marginal effect on regular activity. The

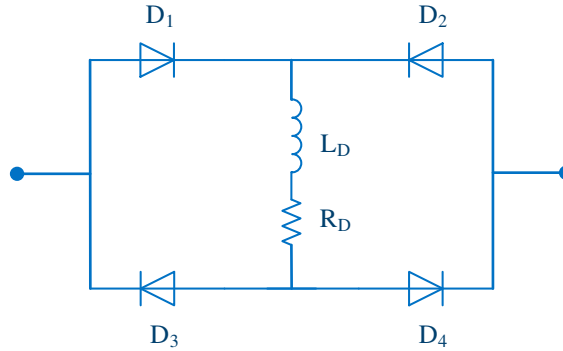


Figure 2.9 Schematic presentation of DC link FCL [55]

reactor can however suppress extreme di/dt efficiently, and can successfully reduce fault current throughout the fault period.

The existing FRT device would not need much control, gate derivation and calculation. The new FRT system has the ability to be quickly applied by the industrial inverter supplier with the least construction work and technical costs. By selecting an acceptable L_d amount, nearly DC current can be achieved for DC reactor.

a comparison of SFCL and SFCLs are presented in “**Table 2.2**” [46].

Table 2.2 Comparison of FCLs

Tracks	SFCL	SSFCL
Steady state loss	Almost zero steady state loss because of the superconductor and it's superconducting state during steady state operation.	Higher steady state loss compared to SFCL but still it's much lower than current limiting reactor.
Interference with neighbouring communication line	It creates interference with transmission line because of the superconducting element.	No interference is created.

Table 2.2 Continued from previous page

Tracks	SFCL	SSFCL
Fault detection	Usually SFCLs don't require additional fault detection mechanism because of the superconductor quenching, superconductor itself can detect fault by detecting critical current, current density, critical temperature etc at the event of a SC fault.	Additional fault detection mechanisms are required to detect SC fault.
Control circuit	Generally no control circuit is required to control the steady state and fault operation.	Control circuit is obvious for all SSFCLs to operate at normal and fault condition.
Recovery time	All SFCLs need a recovery time. Hence they might be vulnerable to multiple instantaneous fault.	No recovery time is required. Almost instantaneous operation.
Implementation status	Many SFCLs have been installed for real field applications in China, USA, Germany, Japan and South Korea. in [19], authors showed that 32 SFCLs were installed in real power system up to 2018.	The number of installed SSFCLs has been reported in [19] is 18 up to 2018. However, feasibility analysis is required to install some of the SSFCL in real system.
Cost	Because of the usage of HTS elements and the refrigeration of HTS elements, the cost is much higher than it's predecessor.	Solid state devices are used in SSFCL, hence cost is low.

2.1.3 Hybrid fault current limiter

Longer recovery time and bulky size, high voltage and high current issues, coordination with conventional relay issue [56], rapid heating of superconductor by multiple quench-

ing [57], economical and technical issues with commercialization and installation [58], [59] are some of the common issues of SFCLs. The aim of hybrid fault current limiter is to focus solving on some of the key issues of SFCLs. The key focus of hybrid fault current limiter is

- to withstand multiple quench without being over heated
- to be compatible with high voltage and current
- to improve in recovery time
- to reduce the superconducting wire size
- to reduce the cost

There are two main ways of building hybrid fault current limiters. First one is: by making a combination of SFCL with SSFCL and second one is: by making internal change in the HTS element and combining existing SFCLs.

2.1.3.1 Non-inductive type hybrid fault current limiter

The non-inductive type hybrid fault current limiter consists of non-inductive coil wound with two types of different HTS wires and a aluminium plate located above the coil. Those two wound different HTS wires kept in opposite direction so that magnetic flux is cancelled together with making inductance of the coil is zero at normal state. At fault state, the difference of index value and critical current of two types of wires results in unequal fault current distribution and a large fault current endured by one wire. This phenomenon leads to the occurrence of inductance which generates the magnetic flux in result. By this way, at the aluminium plate located above the coil the generation of eddy current occur and the repulsive force which pushes up the aluminium plate. This means the opening of fast switch and thus the fault current path is commutated to a resistor. By this principle the fast switch and a hybrid fault current limiter operates [60].

The superconducting non-inductive coil can be wound in two different types such as pancake type or solenoid type. Pancake type has compact volume and a capability of generating higher resistance than solenoid type, this happens because in comparison, pancake reaches higher temperature than solenoid type. However, solenoid type is bigger and it has good insulation characteristics while pancake type has weak insulation characteristic. The advantages of this hybrid fault current limiter is stated below -

- The amount of HTS wire is reduced.
- Comparatively fast recovery time.

- compact size.
- The current limiting impedance value flexible.

2.1.3.2 Bridge type hybrid fault current limiter (BHFCL)

The schematic diagram of bridge type hybrid fault current limiter (BHFCL) shown in “**Fig. 2.10**”. It includes two magnetic devices connected in parallel with one bridge part. The magnetic devices used here are made of Permanent Magnets (PM_s) core material and coils. The bridge part consists of an external reactor (L_f) which limits the fault current and for biasing the cores both DC coils and PM_s are applied. MMF generated by both DC coil and PMs help each other in both magnetic devices. Contrariwise, the upshot of MMF and MMF generated by the AC cycle assist in one magnetic device whereas oppose each other in the other one. More than that, both DC and AC assisting each other by sharing the same coil but having different current path [61].

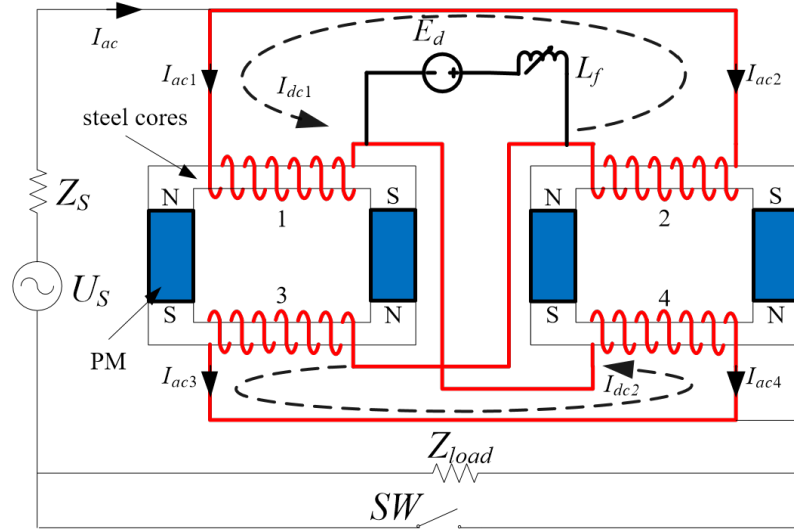


Figure 2.10 Schematic diagram of BHFCL [61]

While operated normally, a deep saturation condition is maintained among all cores in each device for the biasing of DC coils and PMs. Thus, the permeability results in is close to the air and the saturated inductance of each coil is extremely low which is calculated by (2.2).

$$L_s = \frac{n^2}{2(r_m + r_{es})} \quad (2.2)$$

$$L_u = \frac{n^2}{2(r_m + r_{eu})} \quad (2.3)$$

In fault condition, the right sided core comes out of saturation in the positive cycle of the fault current and the left sided iron core comes out of saturation in the negative cy-

cle. As a result, the inductance that remain unsaturated of each coil increased to L_u , alternatively, can be calculated by (2.3). L_f should be much less than unsaturated inductance ($L_f \leq 0.1L_u$) in order to ensure normal operation of the BHFCL. consequently, inductance found in normal and fault condition can be written as L_s and $(2L_s + L_f)$ respectively. Therefore, by choosing an appropriate L_f , fault performance can be designed and guaranteed.

The advantages of BHFCL are -

- The consumption of energy is decreased by using PM.
- The fault clipping performance is ensured by using limiting reactor.
- By sharing AC/DC coils and the compact magnetic device, losses and costs are reduced

2.2 Applications of BFCL

The configuration, advantages, disadvantages applications of SFCLs, hybrid FCLs and SSFCLs are discussed in details in the previous section. In this section application of FCL especially BFCL will be discussed. Fault current limiters are being used in power system primarily for limiting fault current and increasing fault ride through capability and through limiting the fault current at a manageable range it brings stability in the system. FCLs are being used in transmission lines, distribution network [62]–[64], renewable energy sector, transformer and so on. The authors have tested feasibility of a second generation HTS material based SFCL for transmission line application in [65]. In [66], a SFCL has been installed in an extra high voltage transmission line for zero sequence current protection.

Since Our work being based on BFCL, hence this discussion will be limited to the application of BFCL. In the literature we found that a significant amount of works have been carried out for the protection of various types of wind turbines. Generally the fault current level is very high in wind turbine terminals because of the presence of the generator and BFCL plays a very effective role for limiting this high fault current. Another common application of BFCL is to improve the fault ride through (FRT) capability [55], [67]–[69]. A BFCL has been proposed by the authors in [54] for the enhancement of low voltage ride through (LVRT) in a DFIG based wind turbine. The role of BFCL in power grid to enhance stability considering a cyber has been investigated in [70]. This study showed that BFCL is not capable of withstanding cyber-attacks. Transient stability enhancement

of various wind power plants such as doubly-fed induction generator (DFIG) [52], [71], [72], permanent magnet synchronous generator (PMSG) [67], [69], squirrel cage induction generator (SCIG) [73] and self-excited induction generator (SEIG) [74] have been studied extensively with bridge type fault current limiter . Coordination of protective relays with BFCL have been studied in [62], [75], [76].

From the above literature review, it has been clearly demonstrated that the usage of BFCL is very effective in wind farm because of the high fault current level. A bridge type fault current limiter limits fault current, improve fault ride through capability, maintains coordination of protective devices and by doing all these it tends to enhance the stability of the system. However, BFCL is not studied so extensively for other renewable energy sector such as solar farm. Although, the fault current level is comparatively low in a solar system even then using BFCL in a solar system will improve the stability of the system during AC/DC faults.

CHAPTER 3

BFCL MODELLING AND CONTROL

To control the high magnitude of fault current in inverter based distributed generation (IBDG), a controller of bridge type fault current limiter (BFCL) has been proposed in this work. In this chapter a detailed configuration of BFCL, control mechanism and principle of operation have been presented.

3.1 BFCL Configuration

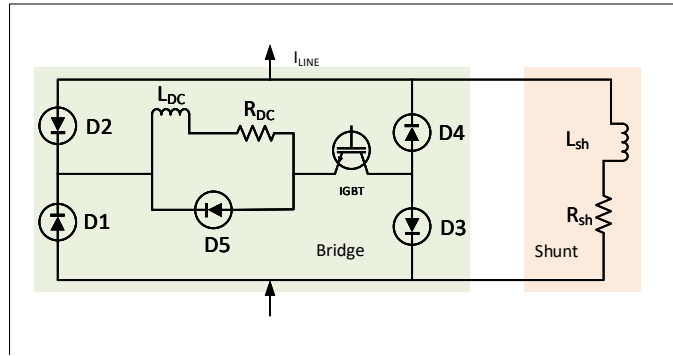


Figure 3.1 BFCL Configuration

In construction basis, BFCL consists of two basic parts stated as the bridge and the shunt as shown in “**Fig. 3.1**” [77]–[79]. BFCL internal parameters are taken depending on the pre-fault power flow [78], [79]. Power consumed by the BFCL after fault can be stated as

$$P_{BFCL} \leq \frac{P_G}{3} \quad (3.1)$$

$$P_{BFCL} = \frac{V_{PCC}^2}{X_{sh}^2 + R_{sh}^2} \quad (3.2)$$

where P_G , V_{PCC} , R_{sh} and X_{sh} are power delivered by the IBDG, voltage at point of common coupling (PCC), shunt resistance and shunt reactance respectively. Equations (3.1) and (3.2) give

$$\frac{P_G}{3} \geq \frac{V_{PCC}^2 R_{sh}}{X_{sh}^2 + R_{sh}^2} \quad (3.3)$$

$$X_{sh}^2 + R_{sh}^2 \geq \frac{3V_{PCC}^2 R_{sh}}{P_G} \quad (3.4)$$

$$R_{sh}^2 \geq \frac{3V_{PCC}^2 R_{sh}}{P_G} - X_{sh}^2 \quad (3.5)$$

$$R_{sh}^2 \geq \frac{3V_{PCC}^2 R_{sh} - P_G X_{sh}^2}{P_G} \quad (3.6)$$

$$R_{sh}^2 P_G \geq 3V_{PCC}^2 R_{sh} - P_G X_{sh}^2 \quad (3.7)$$

$$0 \geq -R_{sh}^2 P_G + 3V_{PCC}^2 R_{sh} - P_G X_{sh}^2 \quad (3.8)$$

$$0 \leq P_G R_{sh}^2 - 3V_{PCC}^2 R_{sh} + P_G X_{sh}^2 \quad (3.9)$$

Taking R_{sh} as the variable and solving the quadratic equation of (3.9) gives

$$R_{sh} \geq \frac{3V_{PCC}^2 \pm \sqrt{9V_{PCC}^4 - 4P_G^2 X_{sh}^2}}{2P_G} \quad (3.10)$$

Omitting minus we get

$$R_{sh} \geq \frac{3V_{PCC}^2 + \sqrt{9V_{PCC}^4 - 4P_G^2 X_{sh}^2}}{2P_G} \quad (3.11)$$

To get a real value of R_{sh} the discriminant of (3.9) should be greater than 0, which gives

$$0 < 9V_{PCC}^4 - 4P_G^2 X_{sh}^2 \quad (3.12)$$

$$X_{sh}^2 > \frac{9V_{PCC}^4}{4P_G^2} \quad (3.13)$$

$$X_{sh} < 1.5 \frac{V_{PCC}^2}{P_G} \quad (3.14)$$

An IGBT switch (CM200HG-130H) plays the key role of the bridge part along with two small DC reactance (R_{DC}) and DC limiting reactor (L_{DC}) and a diode rectifier. The shunt part is build with a shunt resistance and reactance ($R_{sh} + j\omega L_{sh}$) which are connected in

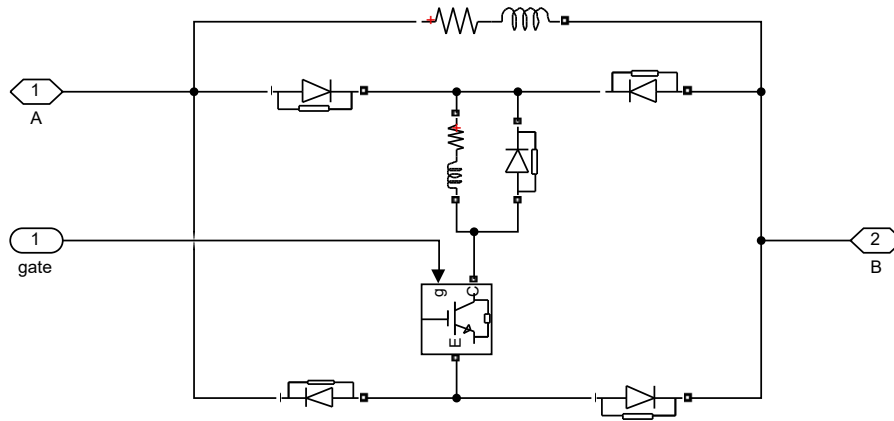


Figure 3.2 BFCL model in Simulink

series to each other. The shunt part is connected with the bridge part in parallel fashion. When fault occurs BFCL inserts the shunt impedance to resist the over current through the line. BFCL is more cost-effective than most other fault current limiting devices since it does not require superconductive materials and characteristics. The control mechanism of the BFCL is stated in the next section.

3.2 BFCL Control Mechanism

The control mechanism of BFCL primarily depends on the control of the IGBT more specifically controlling of the gate pulse of the IGBT. Control circuit of the IGBT is shown in “**Fig. 3.3**”. Here the inverting terminal of the comparator is connected with V_{PCC} and non inverting terminal is connected with a preset threshold voltage V_T . Comparator compares this two voltage and give an output. Depending on the output being ‘High’ or ‘Low’ a ‘Low’ or ‘High’ step voltage is generated respectively for the gate pulse of the IGBT. As long as the gate pulse remains ‘High’ IGBT remains turned **On** and for the gate pulse being ‘Low’, the IGBT is **Off**.

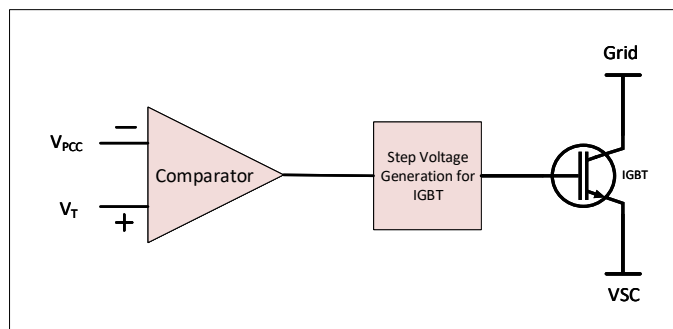


Figure 3.3 Control circuit of the BFCL

During the normal operating condition, the inverting terminal of the comparator which

is connected with V_{PCC} is greater than the non-inverting terminal V_T , hence the output of the comparator is 'Low'. Because of the 'Low' output of the comparator, the step volt-

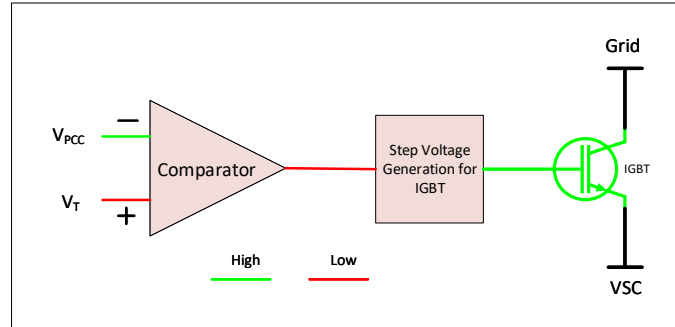


Fig. 3.4.a Normal condition

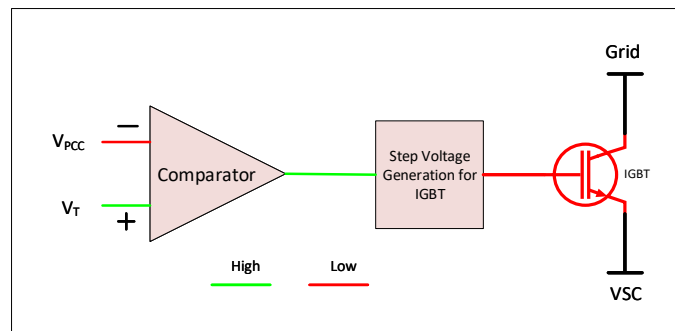


Fig. 3.4.b Fault condition

Figure 3.4 BFCL control mechanism

age generator initiates the IGBT to turn on as shown in “**Fig. 3.4.a**”. “**Fig. 3.4.b**” shows the fault condition mechanism of the control circuit. When fault occurs, V_{PCC} losses its magnitude immediately and V_T , which is the non inverting terminal of the comparator becomes greater than the inverting terminal V_{PCC} . When non-inverting terminal becomes greater than inverting terminal, comparator output also ‘High’ which makes the step voltage generator to give ‘Low’ pulse at the gate terminal of the IGBT. After getting ‘Low’ pulse at the gate terminal, IGBT turns off making the bridge circuit open as shown in “**Fig. 3.7**”.

3.3 BFCL Operation

The principle of operation of BFCL depends on the control of the IGBT switch of the bridge circuit as described in the previous section. Based on the normal condition and fault condition of the grid the principle of operation have been discussed in two parts.

1. Operation at normal condition
2. Operation at fault condition

3.3.1 Operation at normal condition

At the time of normal operation, the IGBT switch comes to conduction hence the shunt part act as an open circuit because of the high impedance of $(R_{sh} + j\omega L_{sh})$ as shown in “**Fig. 3.5**”. Hence Current conducts thorough the bridge circuit.

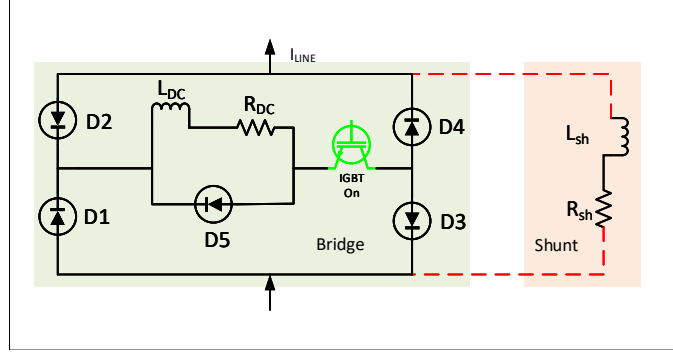


Figure 3.5 BFCL during normal operation

For the positive half-cycle current conduction happens through $D_1 \rightarrow L_{DC} \rightarrow R_{DC} \rightarrow D_4$ as demonstrated in “**Fig. 3.6.a**”. The green line indicates the current path. At the time of negative half-cycle the current follows the path through $D_2 \rightarrow L_{DC} \rightarrow R_{DC} \rightarrow D_3$ as demonstrated in “**Fig. 3.6.b**”.

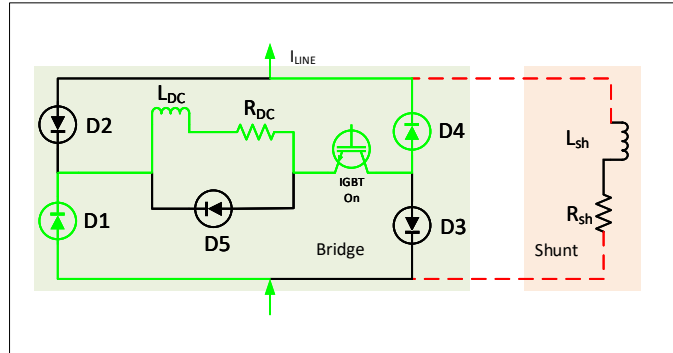


Fig. 3.6.a Positive half cycle

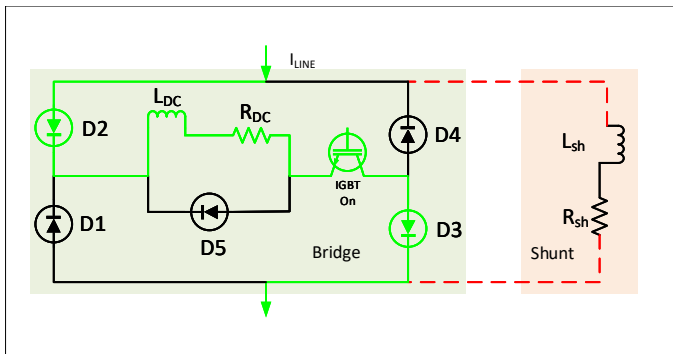


Fig. 3.6.b Negative half cycle

Figure 3.6 BFCL operation at normal condition

3.3.2 Operation at fault condition

When a fault occurs, the control circuit turns off the IGBT switch making the bridge non-functional which has been shown in “**Fig. 3.7**”. At this point, the shunt part of the BFCL

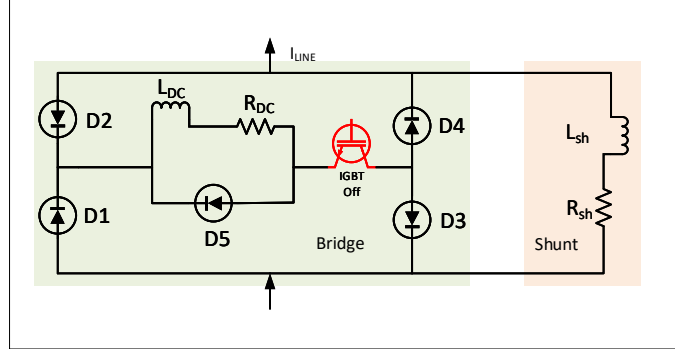


Figure 3.7 BFCL during faulty operation

is the only current path which adds the high impedance ($R_{sh} + j\omega L_{sh}$) in the circuit to limit the fault current. The current path for both positive and negative half-cycle has been shown in “**Fig. 3.8.a**” and “**Fig. 3.8.b**” respectively.

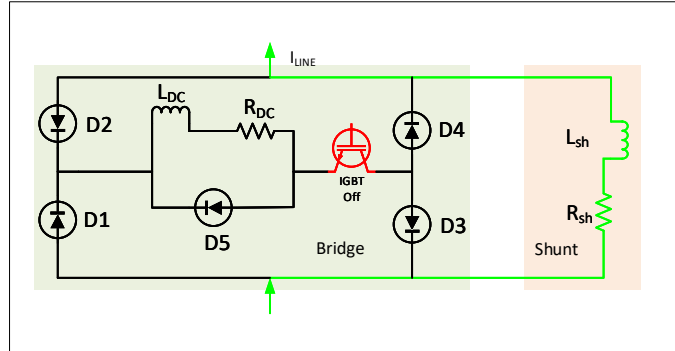


Fig. 3.8.a Positive half cycle

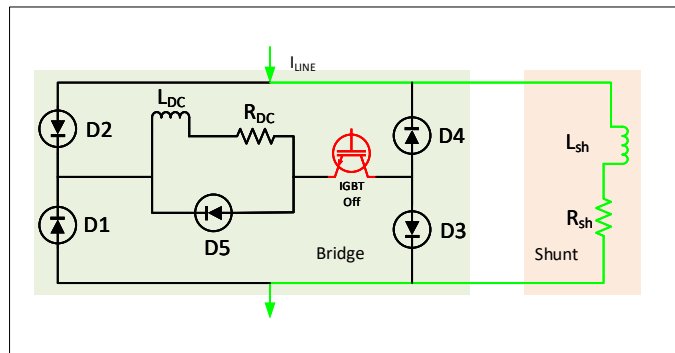


Fig. 3.8.b Negative half cycle

Figure 3.8 BFCL operation at faulty condition

CHAPTER 4

SYSTEM MODELLING AND CONTROLLER DESIGN

4.1 IBDG System Modelling

The proposed system is designed in MATLAB/Simulink. A simplified diagram of the inverter based distributed generation system is shown in “**Fig. 4.1**” as a MATLAB/Simulink block without the bridge type fault current limiter . Blue blocks are the controller subsystem. The inverter based distributed generation is connected to the voltage source converter (VSC), the gate signal of the VSC is provided by the main controller which is shown in “**Fig. 4.2**”. VSC is connected to the grid. Fault is applied between the grid and the VSC. Measurement and transformation subsystem is used to perform the abc to dq conversion of the voltage and current which is supplied to the controller for the controlling of the system. Measurement and transformation subsystem takes it's from the grid. The main controller is a combination of 3 controllers as shown in “**Fig. 4.2**”. A DC link capacitor is connected in parallel with the distributed generator (DG) which is also connected in parallel with the voltage source converter (VSC) to run the VSC properly because the capacitor voltage needs to be regulated in a predefined value to run the VSC properly. VSC converts the DC component into AC and it is connected with the grid through BFCL for the protection of the IBDG system and limiting the fault current.

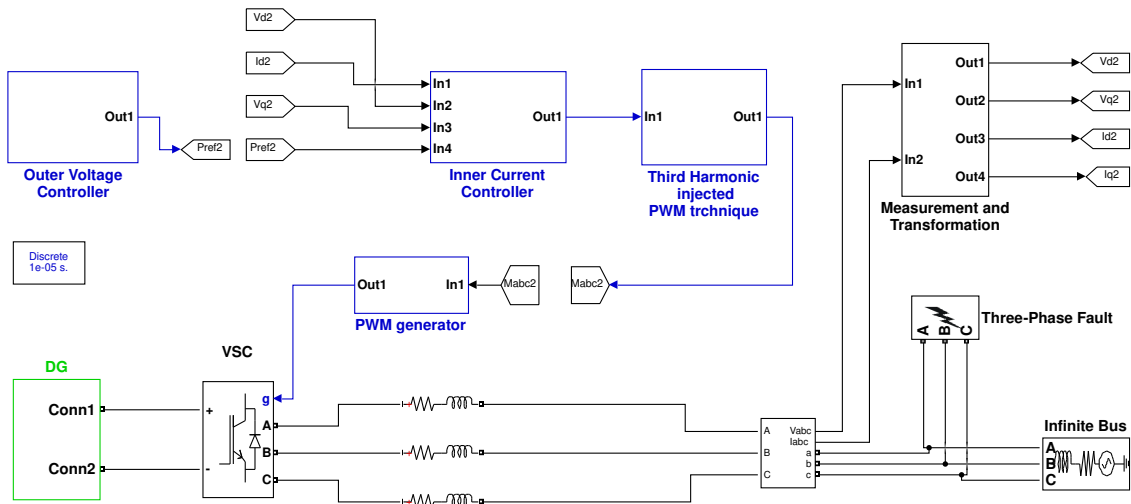


Figure 4.1 Block model of the system in Simulink

Through correctly controlling VSC, the amount of power provided by distributed generator (DG) is transmitted to the grid in such a manner that the power shared between DC

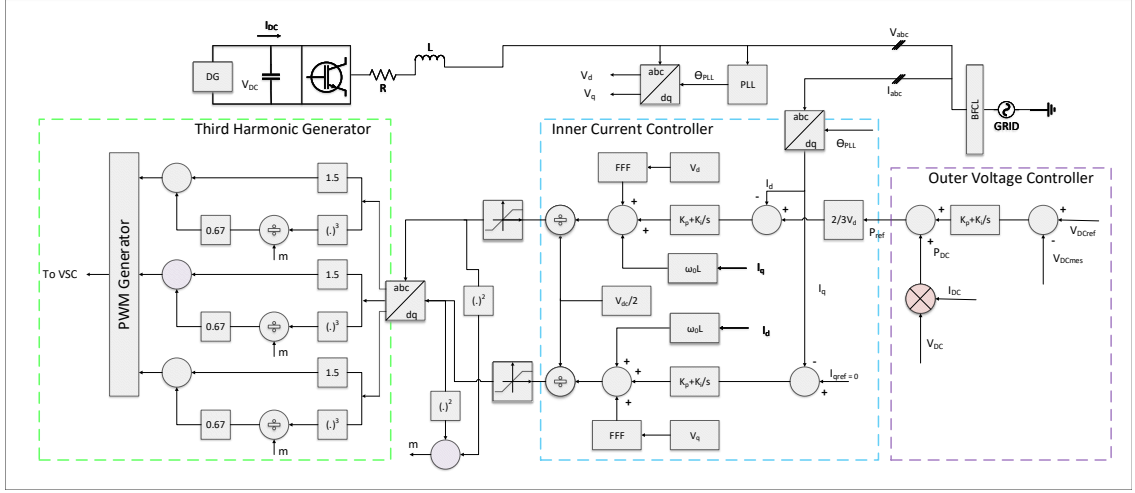


Figure 4.2 Proposed system and controller structure

capacitor and grid is zero. The reference DC link voltage is compared with measured one to process the error with proportional integral (PI) controller. Then, the output of the PI controller is added with the power exchange between DG and the grid to generate the reference power for the VSC .

4.2 Controller Design

The IBDG controller has been proposed to control the active and reactive power as well as to track the DC link voltage of the system. Outer voltage controller, inner current controller and the third harmonic generator are the three main parts of the controller. The active and reactive power of the system can be expressed as follows

$$P_s = \frac{3}{2} V_d I_d \quad (4.1)$$

$$Q_s = -\frac{3}{2} V_d I_q \quad (4.2)$$

“Equation (4.1) and (4.2)” show that controller for active and reactive power must be independent and different in which active power is controlled by d-axis current and reactive power is controlled by q-axis current. The working principle of the each parts of the controller is described in independently in the upcoming subsections.

4.2.1 Outer Voltage Controller

The function of the outer voltage controller is to control the DC voltage. The measured DC voltage (V_{DCmes}) is compared with the reference DC voltage (V_{DCref}) as shown in “Fig. 4.3”. This is possessed by proportional integral controller (PI controller) which is

shown as $K_p + K_i/s$. We get the DC power (P_{DC}) as the product of the DC voltage (V_{DC}) and DC current (I_{DC}). The amount of power given by the voltage controller is added with the DC power (P_{DC}) given by the DG which gives the total power. This total power goes to the inner current controller and it is the reference power (P_{ref}) for the inner current controller.

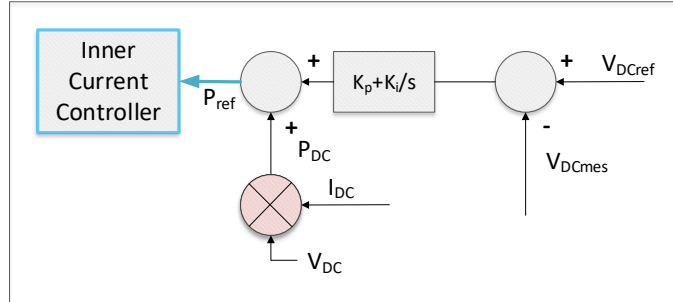


Figure 4.3 Outer voltage controller

4.2.2 Inner Current Controller

Inner current controller has two parts denoted as direct axis current controller and quadrature axis current controller as shown in “**Fig. 4.4**”. Outer voltage controller gives P_{ref} to the inner current controller, inner current controller use this P_{ref} as the input and convert this reference power into direct axis current (I_d) and quadrature axis current (I_q). The

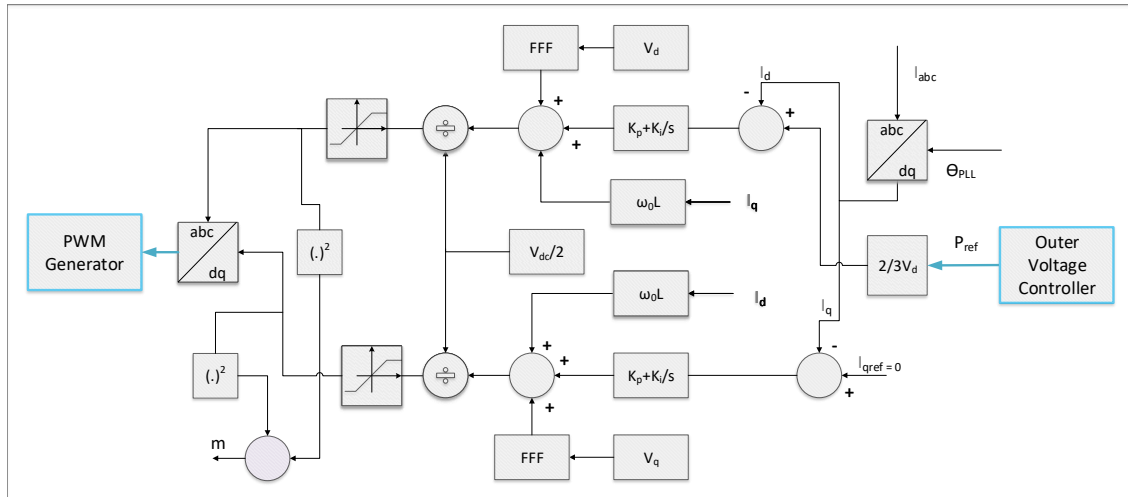


Figure 4.4 Inner current controller

main function of the inner controller is to control the real and reactive power by controlling the direct axis and quadrature axis current respectively since current and power are directly proportional to each other. In this controller quadrature axis current (I_q) is considered 0, which means that the reactive power is controlled as a unity power factor.

Inner controller is actually taking the reference current (I_{dref}) from the outer voltage controller because as shown in “**Fig. 4.4**”, the multiplication factor with P_{ref} is $\frac{2}{3V_d}$ which removes voltage from the reference DC power. Then this current is compared with I_{dmes} which we get from converting the abc component into dq component. Considering the operation being steady state and transformation of abc to dq gives “(4.3), (4.4)”.

$$L \frac{dI_d}{dt} = L\omega_0 I_q - RI_d + V_{td} - V_d \quad (4.3)$$

$$L \frac{dI_q}{dt} = L\omega_0 I_d - RI_q + V_{tq} - V_q \quad (4.4)$$

At the end of the inner current controller the direct axis current and quadrature axis current are again converted into abc component and this abc component goes to third harmonic PWM generator .

4.2.3 Third harmonic injected PWM Generator

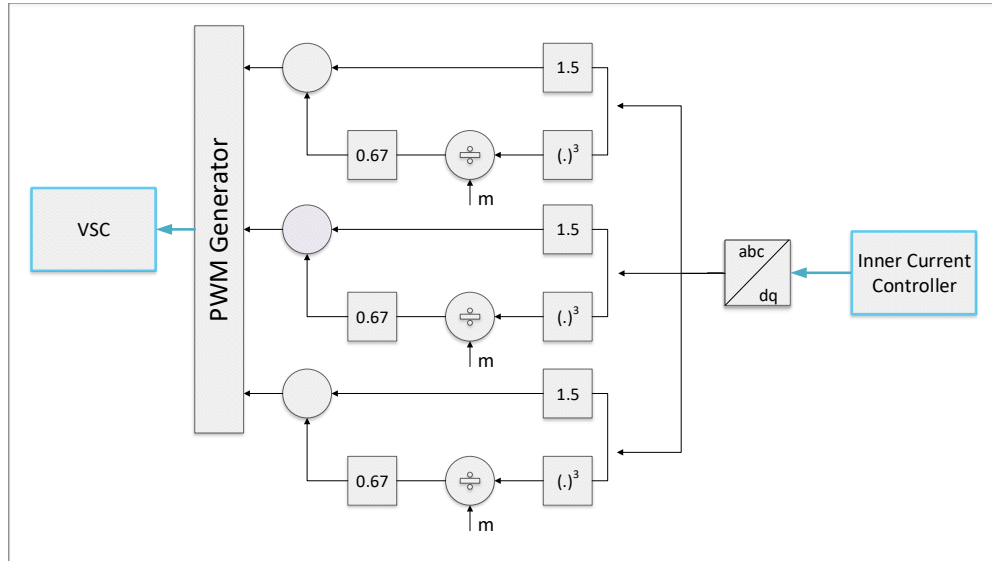


Figure 4.5 Third harmonic injected PWM technique

Third harmonic injected PWM technique is shown as a block diagram in “**Fig. 4.5**”. The VSC controller of “Fig. Fig. 4.2” is established by applying the technique of third harmonic injection along with the “(4.3), (4.4)”. The dq current from the inner current controller is converted into abc component for using the in PWM generator. Third harmonic injected PWM generation technique is used in this work because it requires lesser DC link voltage than other PWM generation technique. The third harmonic PWM generator produces gate pulse then this gate pulse is provided to the VSC.

In a nutshell, the overall operation of the three parts of the controller can be explained as follows -

The outer voltage controller controls the DC voltage and gives the total power output as P_{ref} . This P_{ref} is converted into current in inner current controller and is used as reference direct axis current. The inner current controller controls the power by controlling the dq current. At the end of inner current controller the dq current is again converted into abc current and this current is used in third harmonic PWM generator to produce gate pulse for the VSC.

CHAPTER 5

SIMULATION

The proposed system was simulated in MATLAB/ SIMULINK. The parameters shown in “**Table 5.1**” has been used to simulate the proposed inverter based distributed generation system [53]. The inverter based distributed generation has been simulated for 0.9 second.

Table 5.1 Proposed System Parameter

Parameter	Value
Grid Voltage	480 V (L-L rms)
Frequency	60 Hz
Interface resistor (R)	2.38 mΩ
Interface reactance (L)	200 μH
Equivalent DC bus capacitor	12525 μF
Reference DC bus voaltage	3.0 KV
BFCL resistor	15 mΩ
BFCL inductor	0.25 mH
Inner current controller (kp)	0.2
Inner current controller (ki)	3.26
Outer voltage controller (kp)	0.5
Outer voltage controller (ki)	10
Feed forward function (FFF)	$\frac{1}{1 + 8.6 \times 10^{-6}s}$

Initially, the DC link capacitor is charged up to 1.042 KV by keeping both inner and outer controller turned off. Then inner current controller and outer voltage controller are turned on and the DC link voltage is set to 2 KV at 0.15 seconds. At 0.35 seconds the inverter based distributed generation system gains its stability as shown in “**Fig. 5.3**”. “**Fig. 5.3**” shows the system without any fault being implemented.

Fault between:

☒ Phase A ☒ Phase B ☒ Phase C ☒ Ground

Switching times (s): [0.5 .58] ☐ External

Fault resistance Ron (Ohm): 0.00008

Ground resistance Rg (Ohm): 0.002

Snubber resistance Rs (Ohm): 1e6

Snubber capacitance Cs (F): inf

Measurements: None

Figure 5.2 Fault block parameters in SIMULINK

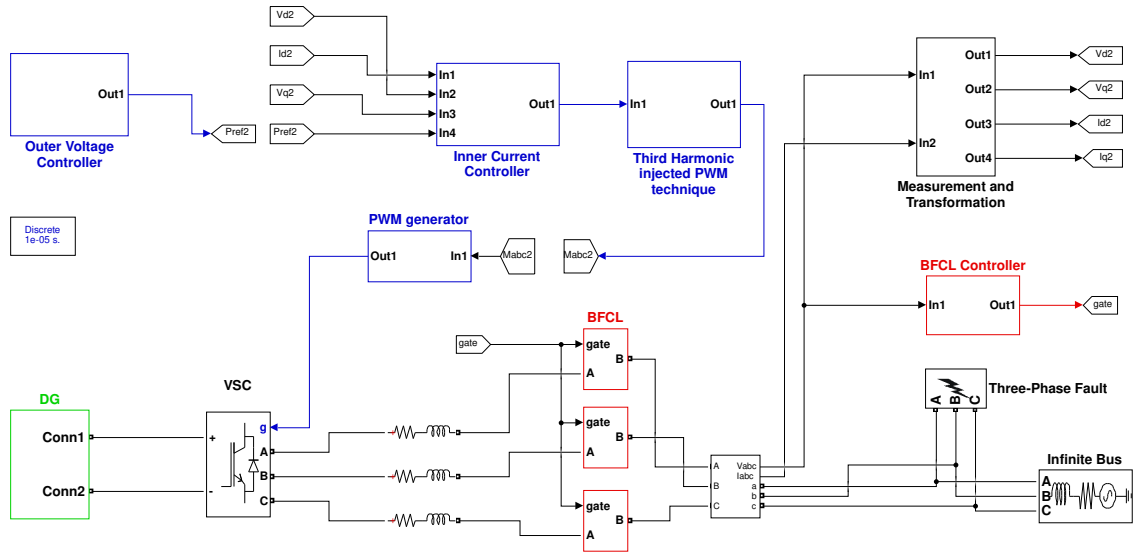


Figure 5.1 Simulation model of the system with 3 BFCL in 3 phase

After inverter based distributed generation system gains stability, balanced and unbalanced faults are applied in the system. For this simulation a 3LG fault is implemented in the system at 0.5 second and fault duration in the system is up to 0.58 second as shown in “**Fig. 5.2**”. After the end of fault duration at 0.58 second, the inverter based distributed

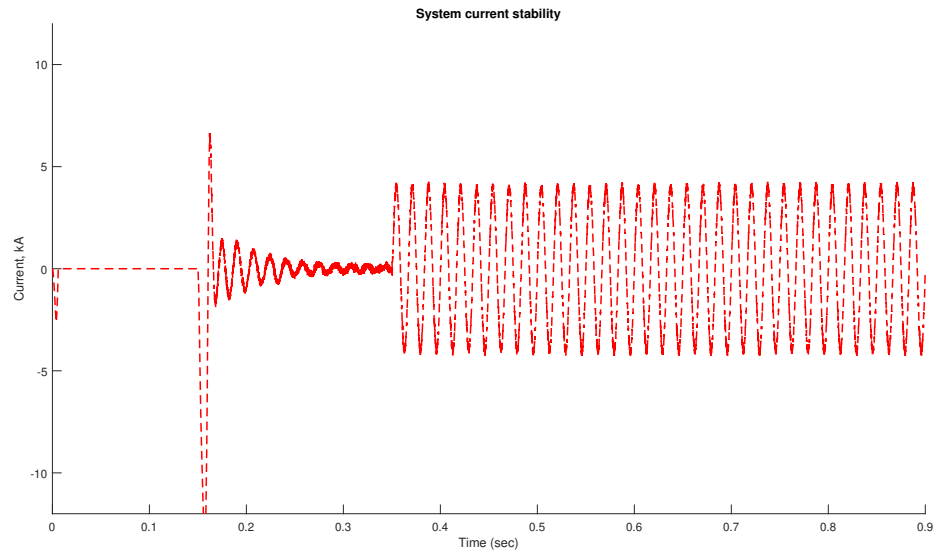


Figure 5.3 System gains stability at 0.35 second

generation system starts to gain stability immediately and the simulation ends at 0.9 second.

5.1 BFCL during simulation

BFCL operation during normal and fault conditions are explained in details in chapter 3. Now, the simulation results are given here. The operation of the bridge type fault current limiter has been controlled by the controller circuit of bridge type fault current limiter which has been demonstrated in “Fig. 3.4.a” and “Fig. 3.4.b”. To explain the operation the figures are stated here again in “Fig. 5.4.a” and “Fig. 5.4.b”. During the

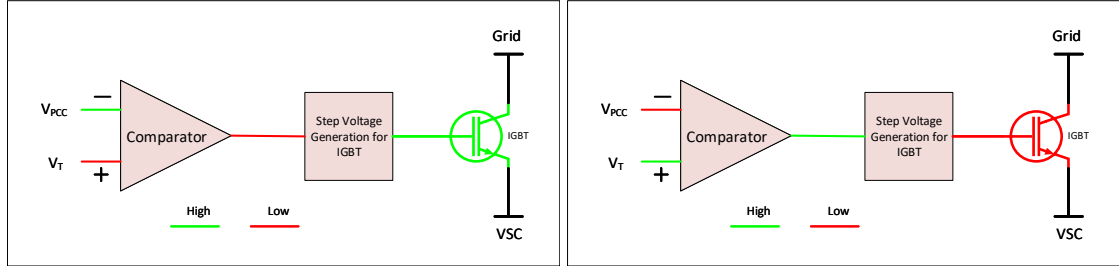


Fig. 5.4.a Normal condition

Fig. 5.4.b Fault condition

Figure 5.4 BFCL control mechanism

normal operation V_{pcc} remains almost constant at 275 V and gate pulse remains High as shown in “Fig. 5.5”. As soon as fault initiates at 0.5 second, the magnitude of V_{pcc} starts to decrease at a very rapid rate as shown in “Fig. 5.5”. Bridge circuit of the bridge type fault current limiter operates normally until fault is implemented following normal operation condition as shown in “Fig. 3.6.a” and “Fig. 3.6.b”. After V_{pcc} decreases lower

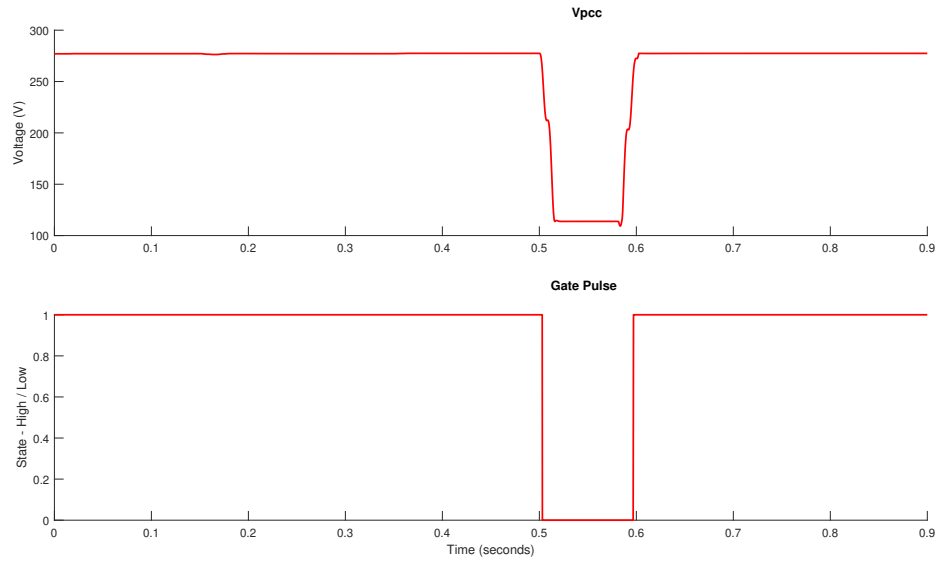


Figure 5.5 V_{pcc} and IGBT gate pulse during fault

than 260 V which is the predefined value of V_T set in the comparator of the BFCL control

circuit which has been explained in “**Fig. 5.4.b**”, comparator output becomes high hence step voltage generator for the IGBT produces Low pulse as shown in “**Fig. 5.5**”.

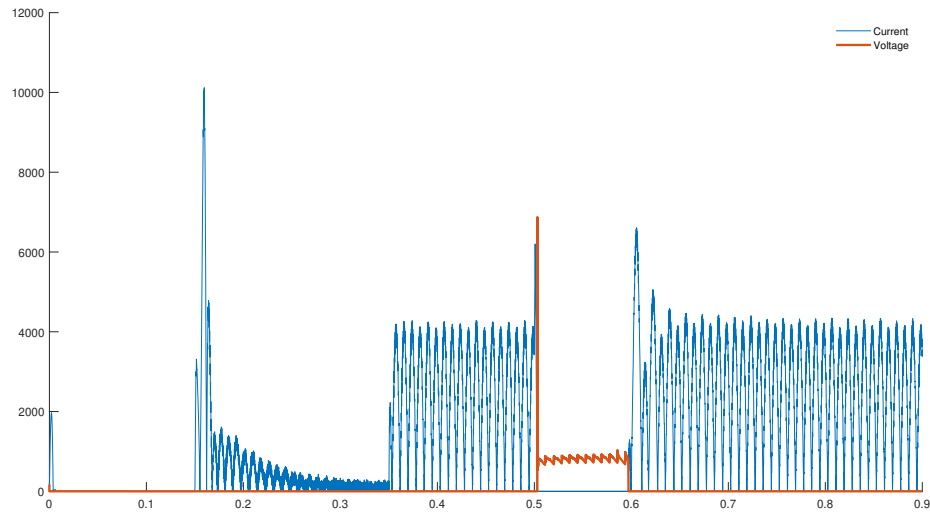


Figure 5.6 Current and voltage across BFCL IGBT

After the gate pulse becomes Low IGBT turns off. Current and voltage across the IGBT is shown in “**Fig. 5.6**”. It is noticeable that there is no negative current through the IGBT because both positive and negative half cycle pass the IGBT from the same side. As soon as IGBT turns off, the bridge circuit of the BFCL also becomes open, hence to limit the fault current the shunt part of the IBDG becomes active as shown in “**Fig. 3.8.a**”. The shunt part of bridge type fault current limiter becomes active only during the fault

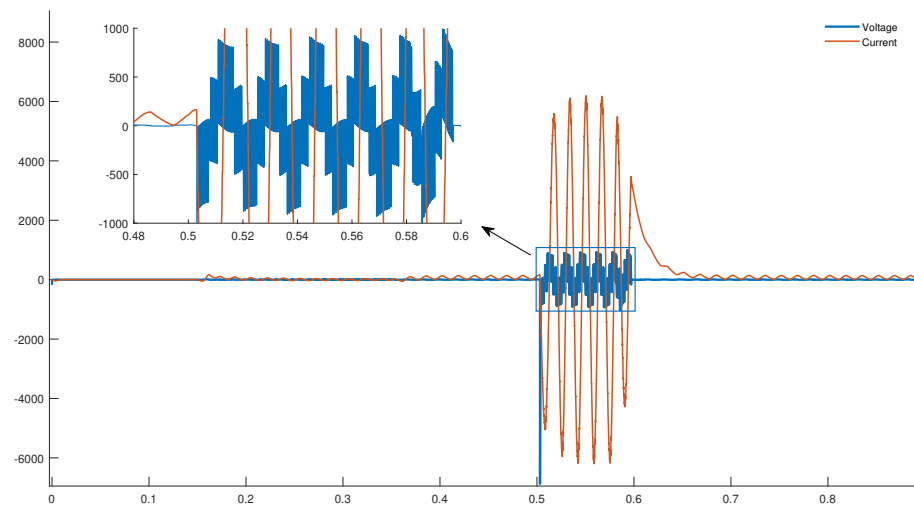


Figure 5.7 Current and voltage across shunt branch of BFCL

operation as shown in “**Fig. 5.7**”. As it is seen in the figure, there is no voltage drop across the shunt branch during the normal operation of the bridge type fault current limiter , but there remains some current whose magnitude is very low compared to the current of the circuit. Also we see, the voltage across the shunt branch becomes almost 0 as soon as the fault finishes at 0.58 second but the current decreases it’s magnitude gradually because of the presence of the inductor in the shunt branch. Inductor releases it’s current gradually, inductor current can’t be zero instantly.

During the normal operation of bridge type fault current limiter for the positive half-cycle current conduction happens through $D_1 - L_{DC} - R_{DC} - D_4$ as demonstrated in “**Fig. 3.6.a**”. The green line indicates the current path. Current through D_1 and D_4 is shown in “**Fig. 5.8**”, during the positive half cycle of normal operation current follows this path. Diode D_1 and D_4 basically are situated at two different places of the same current path, hence the current through the both diodes are same. There is no current through the diodes during fault because IGBT turns off at the time of fault making the bridge circuit open. There is no voltage drop across the diodes during normal operation.

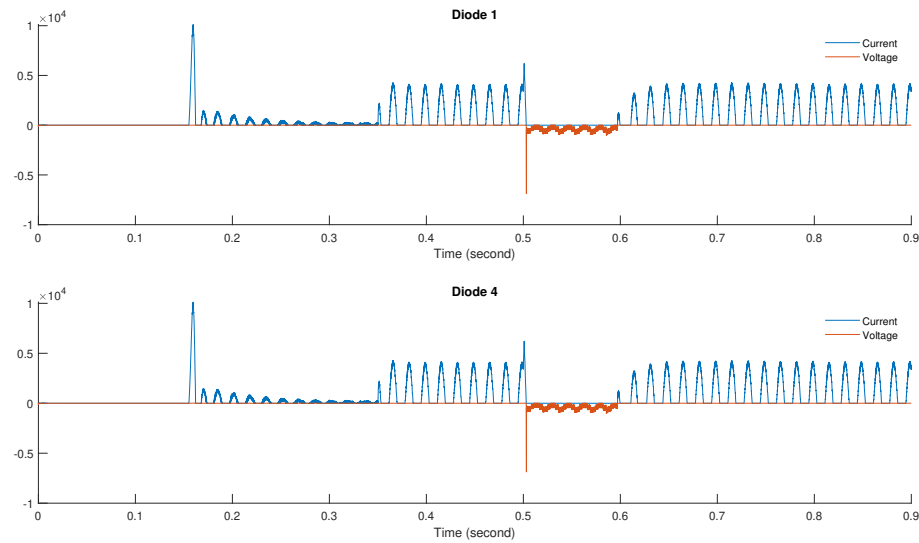


Figure 5.8 Current and voltage across diode D_1 and D_4

At the time of negative half-cycle of the normal operation, the current follows the path through $D_2 - L_{DC} - R_{DC} - D_3$ as demonstrated in “**Fig. 3.6.b**”. Current and voltage across diode D_2 and D_3 is shown in “**Fig. 5.9**”. Although current across all diodes looks similar but they are not similar, during positive half cycle current pass through D_1 and D_4 and during negative half cycle current pass through D_2 and D_3 . For this reason both

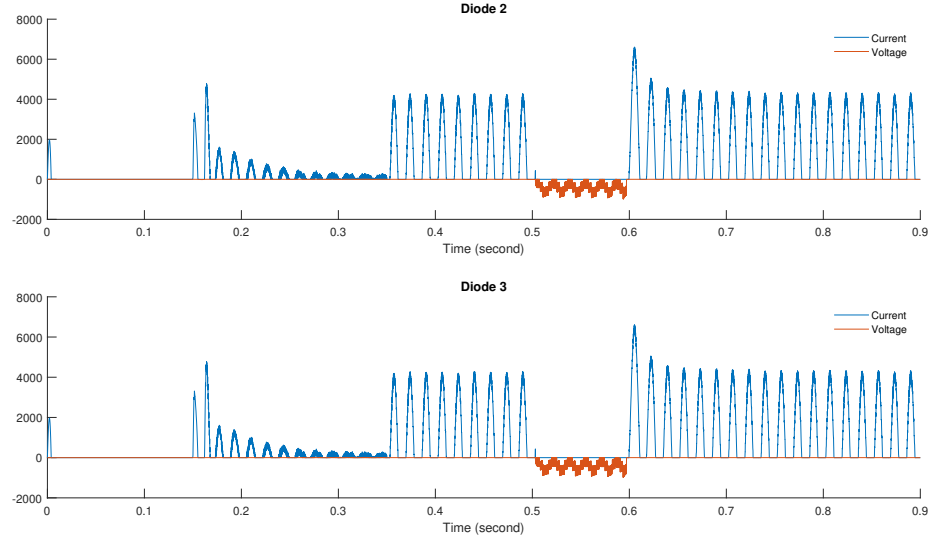


Figure 5.9 Current and voltage across diode D_2 and D_3

“Fig. 5.8” and “Fig. 5.9” show one half of the total current across them. For complete current, combining positive and negative half cycle current gives the result of “Fig. 5.10”.

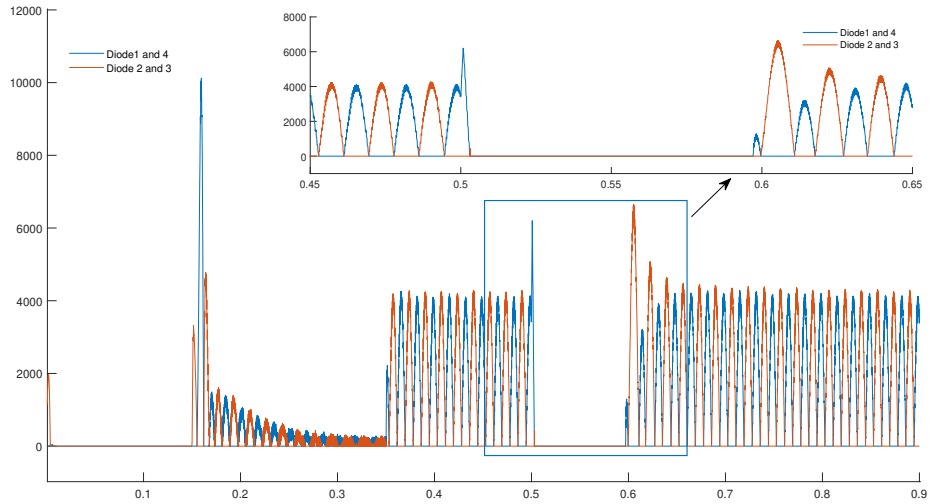


Figure 5.10 Current through Diode D_1 , D_4 , D_2 and D_3

5.2 Controller during simulation

The main controller of the inverter based distributed generation system has been divided into three parts: outer voltage controller , inner current controller and third harmonic PWM generator to explain easily in chapter 4. Here the simulation has also been explained accordingly. Outer voltage controller takes voltage and current from the inverter

based distributed generation and produce power which is used as reference power for inner current controller. Inner controller use power to control the current and controlling current it controls the power. At the end of inner current controller it converts dq current to abc to use in third harmonic PWM generator .

5.2.1 Outer voltage controller

Among the three main parts of the inverter based distributed generation proposed controller outer voltage controller is the smallest and the simplest one. Outer controller supplies reference power to the inner current controller In outer voltage controller The simulated DC voltage (V_{DCsim}) is compared with the reference DC voltage (V_{DCref}) as shown in “**Fig. 4.3**” which is possessed by proportional integral controller (PI controller). The power of th DG is given by the product of DC voltage and DC current. By controlling the voltage, we get the total power denoted as P_{ref} from the outer voltage controller which is shown in “**Fig. 5.11**”.

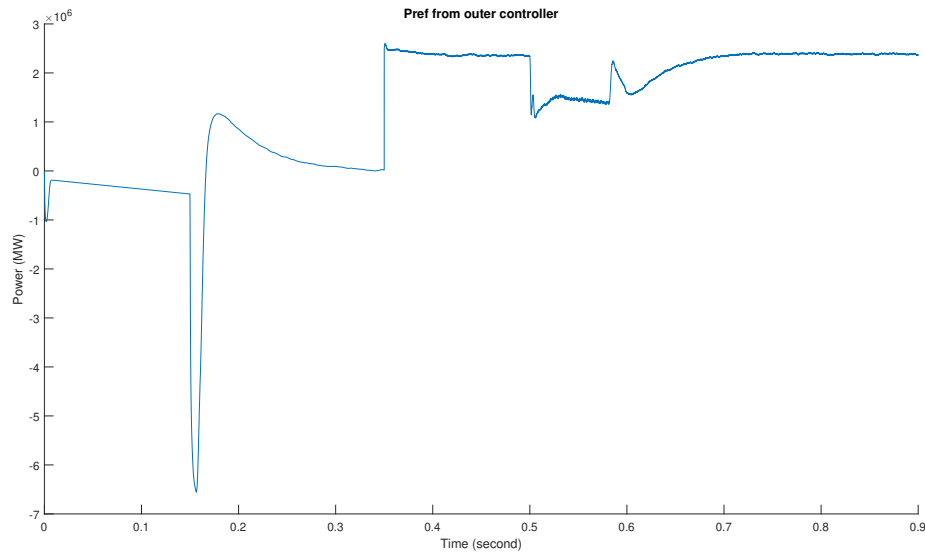


Figure 5.11 Reference power from outer voltage controller

5.2.2 Inner current controller

The reference power P_{ref} plays a key role in the controller, because inner current controller takes this power as the reference power and converts it to current by multiplying it with a factor of $2/3V_d$, where V_d is the direct axis current as shown in “**Fig. 5.12**”. After converting the power P_{ref} into current, inner current controller uses this current as the reference direct axis current is denoted as I_{dref} . abc to dq conversion of the line current

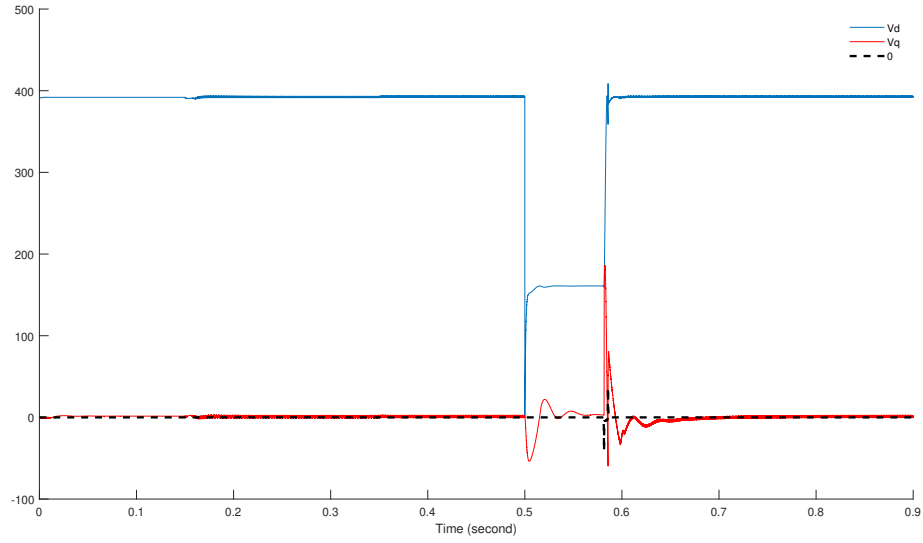


Figure 5.12 abc to dq0 converted line to line voltage

gives us direct axis current and quadrature axis current denoted as I_{dsim} and I_{qsim} . The direct axis current I_{dsim} is compared with I_{dref} which is possessed by PI controller. This is shown in “**Fig. 5.13**”. I_{dref} controls the active power of the inverter based distributed generation system. The quadrature axis current denoted as I_{qsim} is compared with 0 cur-

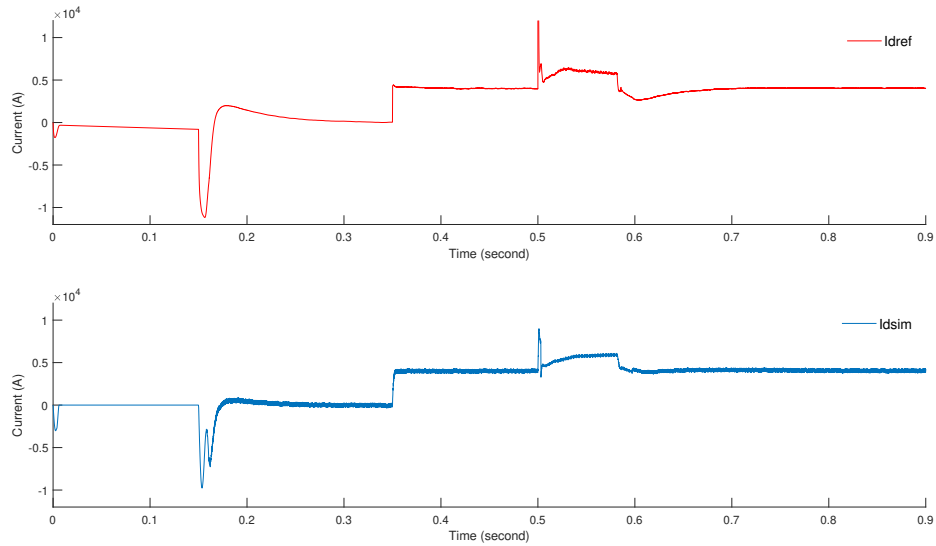


Figure 5.13 I_{dref} and I_{sim}

rent as shown in “**Fig. 5.14**”. I_{qref} is taken as 0 because reactive power is treated as unity power factor. This is also controlled by PI controller. At the end of inner current controller we get the dq0 current as shown in “**Fig. 5.15**”. This direct and quadrature axis current goes to third harmonic PWM generator after getting them converted into abc.

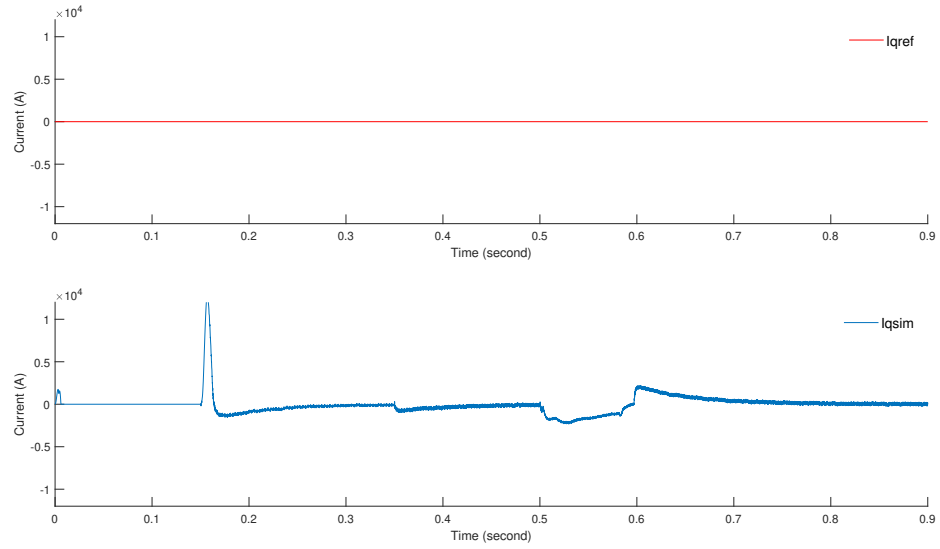


Figure 5.14 I_{qref} and I_{qsim}

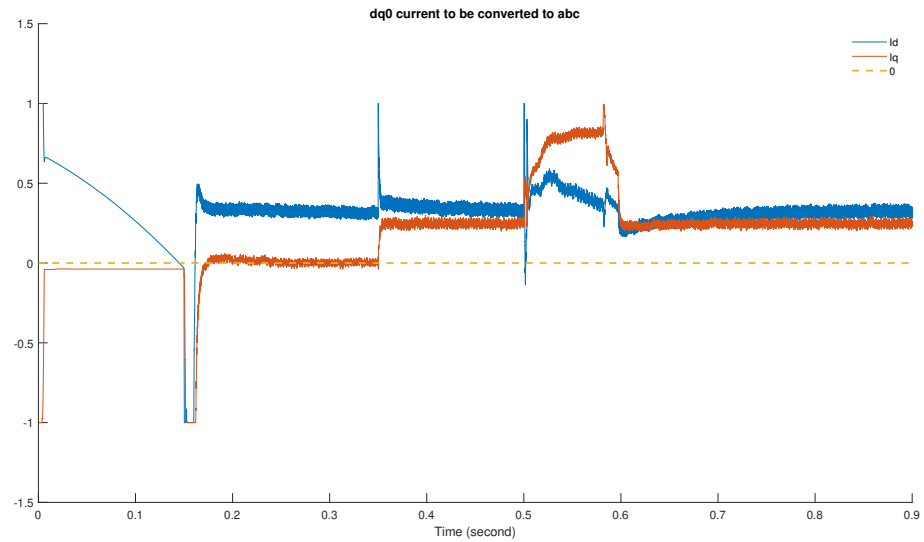


Figure 5.15 dq current at the end of inner current controller

5.2.3 Third harmonic injected PWM generator

Third harmonic PWM generator takes the dq0 current of “**Fig. 5.15**” and convert them into abc component as shown in “**Fig. 5.16**”. Third harmonic PWM generator uses the abc component and produces the output as shown in “**Fig. 5.17**”. This output goes to PWM generator. The frequency of the PWM generator is 1680 Hz.

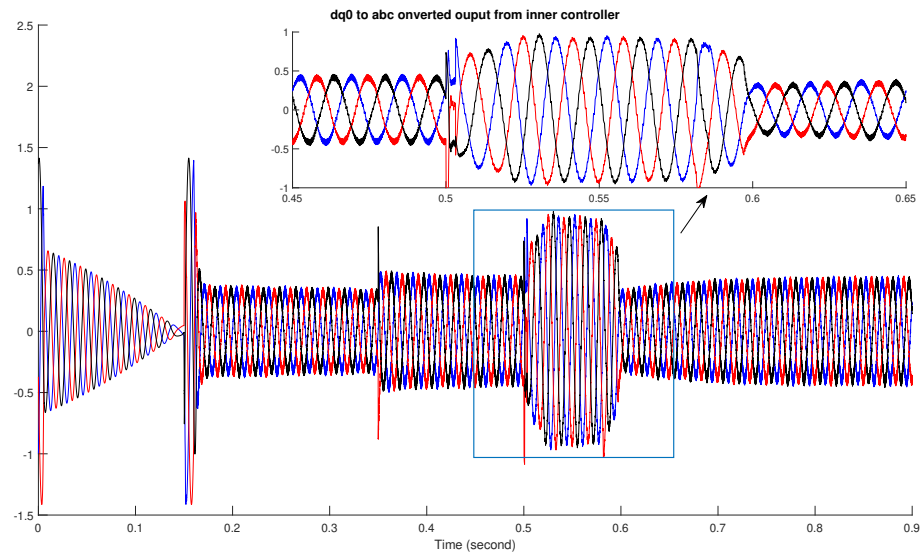


Figure 5.16 dq to abc converted current for third harmonic injected technique

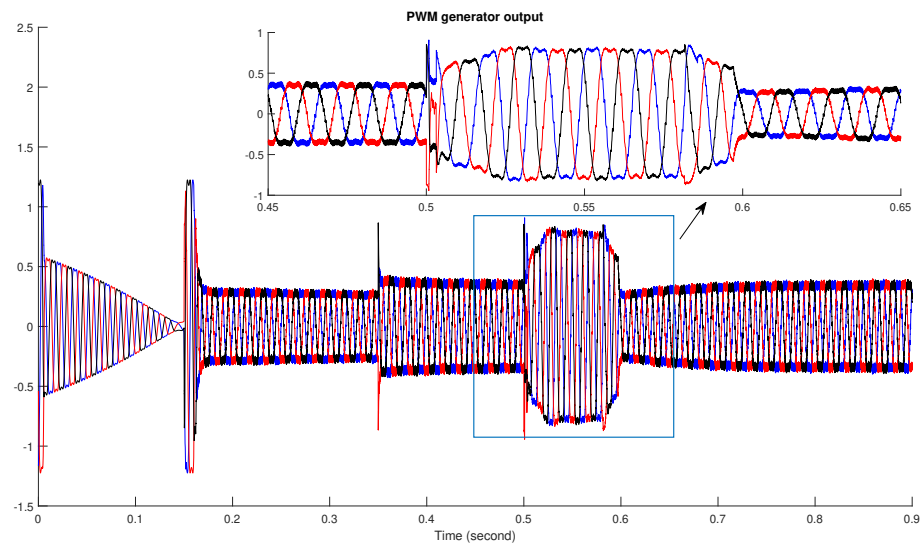


Figure 5.17 Third harmonic injected output for PWM generator

CHAPTER 6

RESULTS AND DISCUSSIONS

In last 5 chapters, literature review, faults effects on power system, BFCL configuration, design and control strategy, system controller design and simulation are discussed in details. Based on the simulation, overall system stability, effectiveness of the controller and various fault current limiting improvement parameters will be discussed in this chapter.

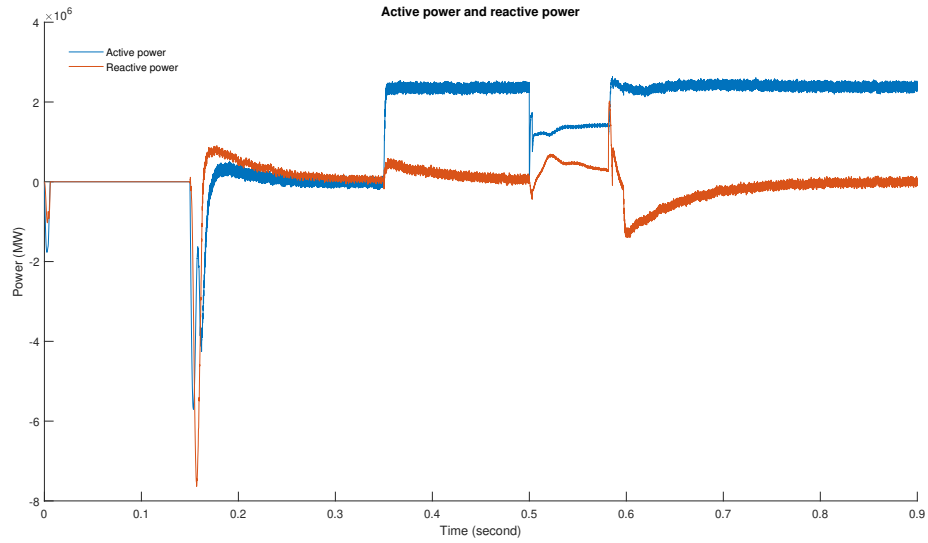


Figure 6.1 Real and reactive power of the system at fault condition

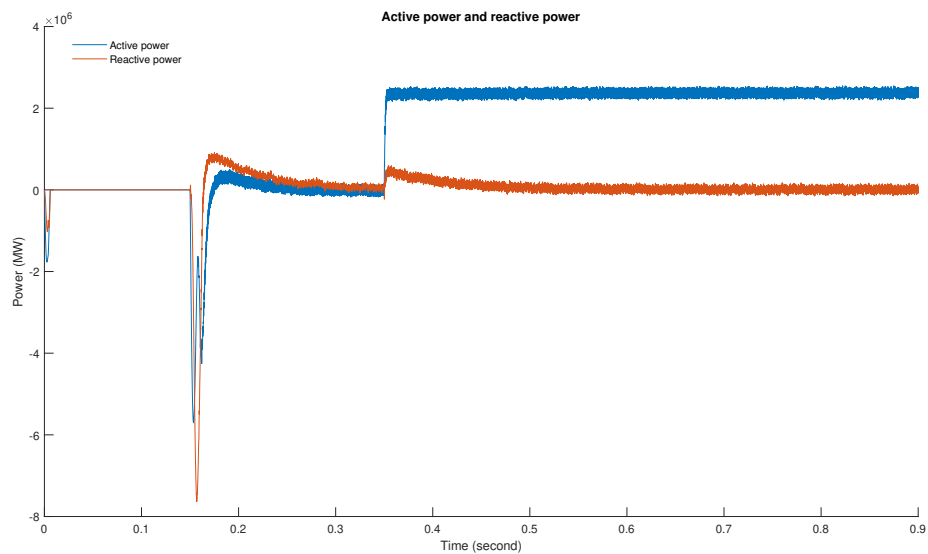


Figure 6.2 Pre-fault real and reactive power of the system

In a power system all power is expected to be real power and try to keep the reactive power as low as possible. The real/active and reactive power of the proposed inverter based distributed generation system is shown in “**Fig. 6.1**”. from the figure, we see that except the fault occurrence time the active power is at good condition and reactive power is almost at zero level. Active and reactive power of the system at pre-fault or steady state condition is shown in “**Fig. 6.2**”, from where we see the complete scenario of active and reactive power of the system.

6.1 Reference Tracking of the System

The reference power and the simulated power are compared in “**Fig. 6.3**”. It is well demonstrated that system power is completely following the reference power which proves that the control system we have designed is good at tracking the reference of the system. The reference DC voltage and simulated DC voltage are compared in “**Fig. 6.4**”. We see that system DC voltage gets stable at 0.35 second.

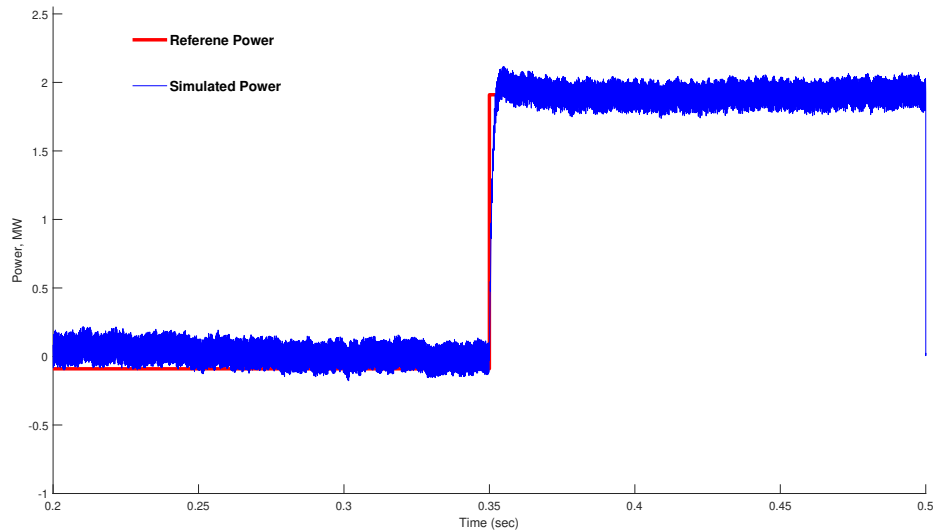


Figure 6.3 Improvement in reference power tracking

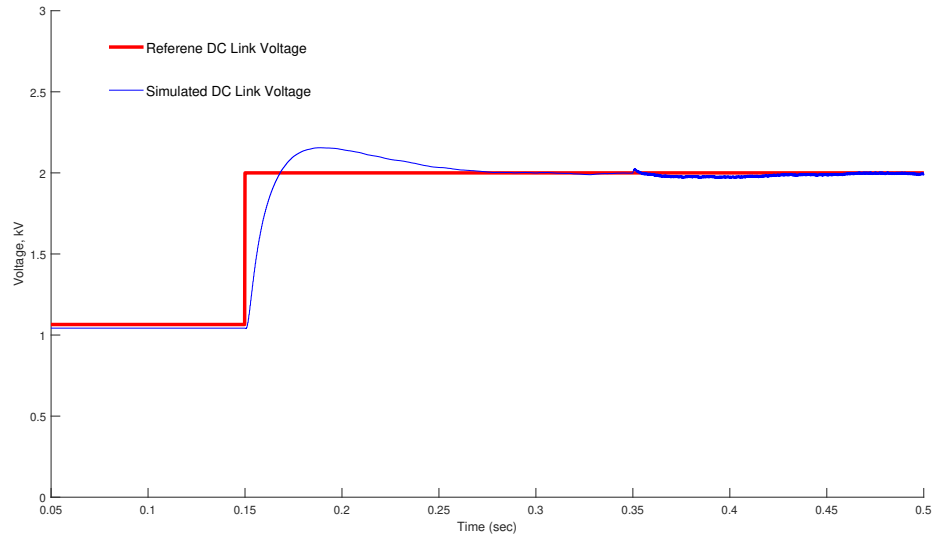


Figure 6.4 Improvement in reference voltage tracking

6.2 Fault Current Limiting Performance

The primary focus of this work is to study the fault current limiting performance in an inverter based distributed generation system for it's protection from high fault current. To

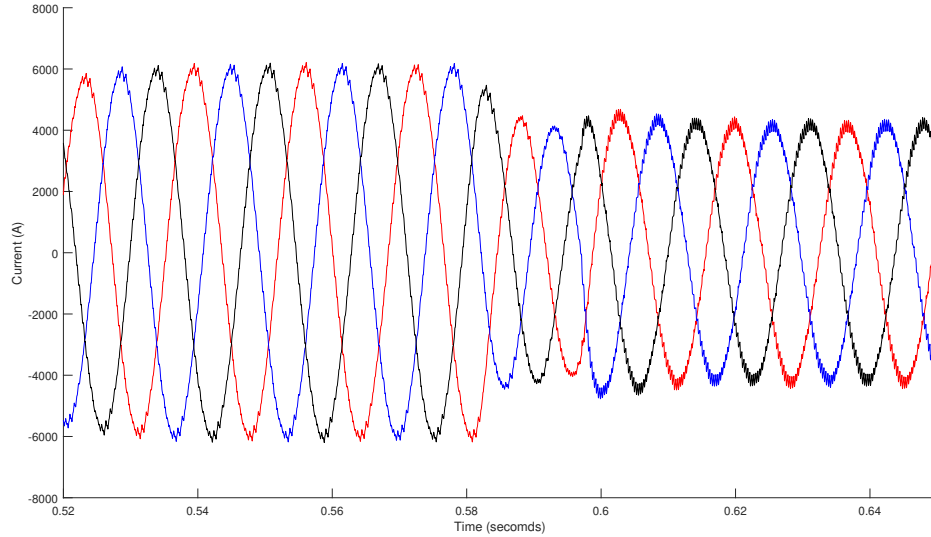


Figure 6.5 Limited fault current with BFCL during a 3lg fault

do that, We have applied symmetrical and unsymmetrical fault in the system and studied the fault condition in three different scenarios.

1. No protection/ no FCL
2. Protection with SDBR
3. Protection with BFCL

Instead of 3 phases we have taken a single phase to demonstrate the result and to compare so that it can be demonstrated well. However, a 3 phase representation of limited fault current with BFCL at the occurrence of a 3lg fault is shown in “**Fig. 6.5**”. A comparison of fault current limiting capability of the 3 scenarios is shown in “**Fig. 6.6**”. The fault current is maximum with no FCL which is expected and BFCL limits it at a good extent. Another noticeable thing is BFCL limits the fault current at the very beginning of the fast cycle.

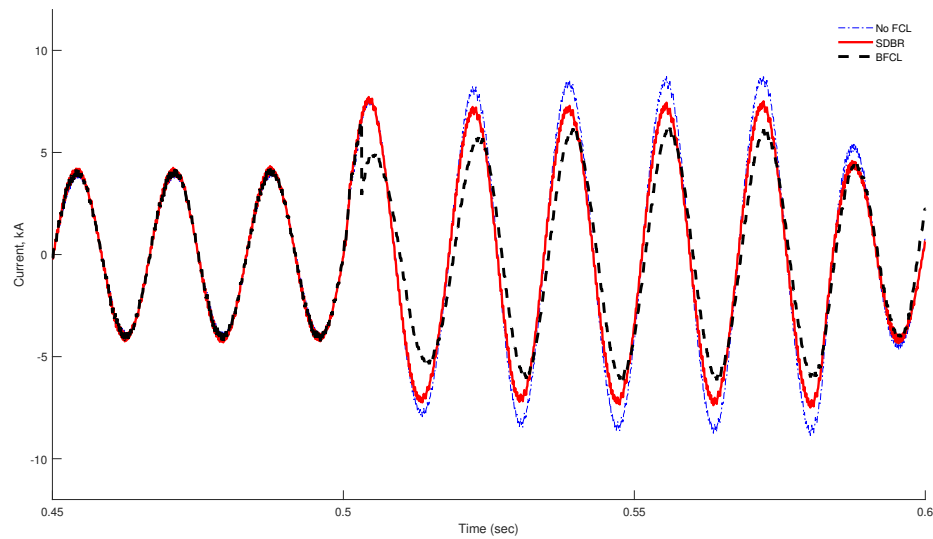


Figure 6.6 Limited 3lg fault current

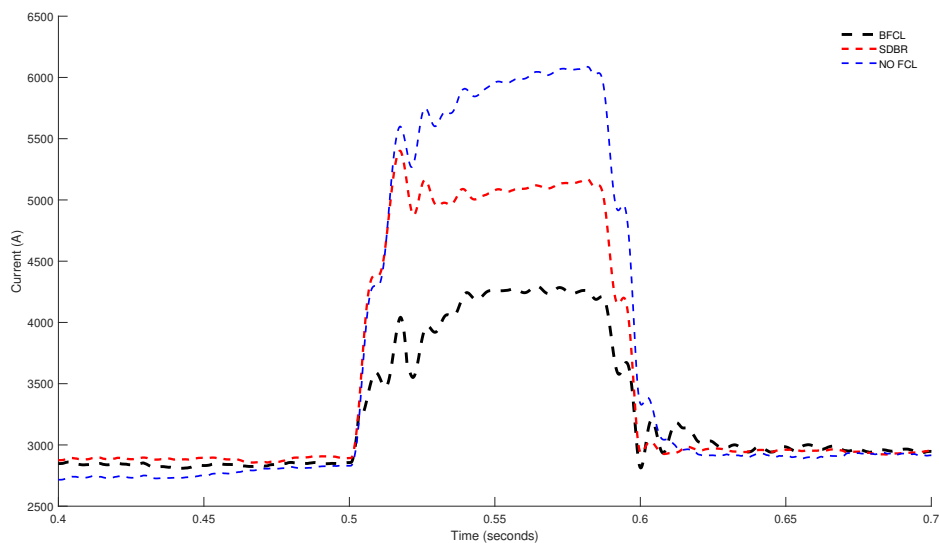


Figure 6.7 RMS current during 3LG fault

RMS value of the fault current during the 3LG fault is demonstrated in “**Fig. 6.7**”. The

RMS values presents a better visualization of the fault current limiting capability of BFCL.

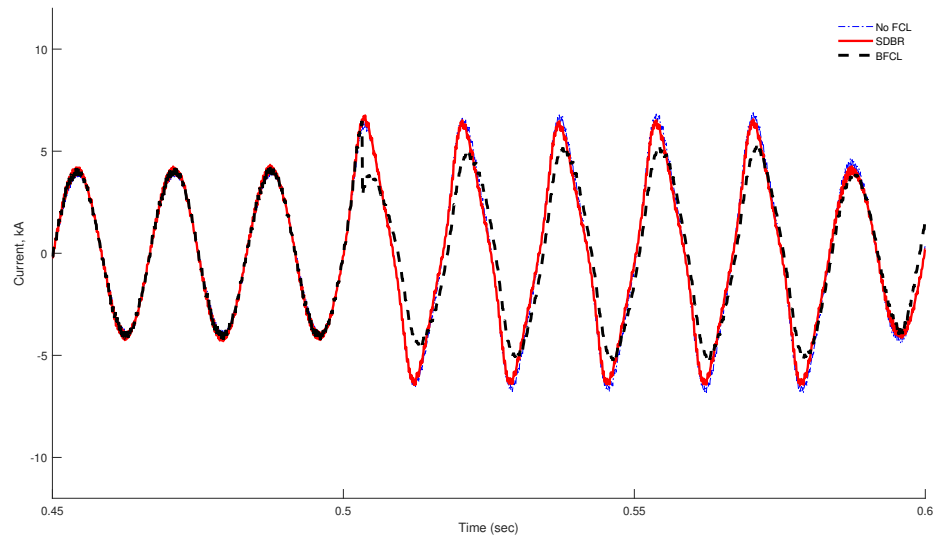


Figure 6.8 Limited 2LG fault current

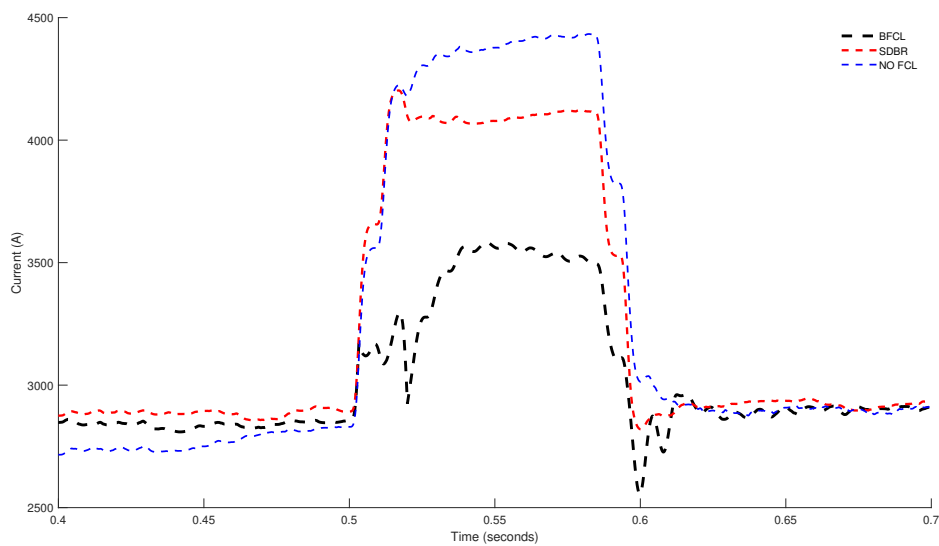


Figure 6.9 RMS current during 2LG fault

For unsymmetrical 2LG fault, current comparison is shown in “**Fig. 6.8**”, and RMS currents is shown in “**Fig. 6.9**”. Current limiting capability of SDBR isn’t very significant during the 2lg fault. But BFCL limits the fault current well as seen from both of these figures.

A numerical representation of fault current in all 3 frameworks based on BFCL, SDBR

and No FCL has been shown in “**Table 6.1**”. It is seen that 3LG fault current is about 6.2 kA for BFCL which is about 7.4 kA and 8.8 kA for SDBR and No FCL respectively. Almost the same degree of increment is seen for 2LG fault.

Table 6.1 Numerical representation of fault current limiting capability of the three frameworks

	3LG FAULT		2LG FAULT	
	Positive peak Current (kA)	Negative peak Current (kA)	Positive peak Current (kA)	Negative peak Current (kA)
No FCL	8.77	8.87	6.88	6.84
SDBR	7.42	7.4	6.44	6.44
BFCL	6.21	6.1	5.19	5.26

“**Table 6.2**” shows the percentage improvement of fault current limiting capability of BFCL over other two frameworks. BFCL makes almost 25 to 30 % improvement over no protection scenario and 15 to 20 % improvement over SDBR in terms of fault current limiting.

Table 6.2 Percentage Improvement of BFCL in fault current limiting capability

	3LG FAULT		2LG FAULT	
	Positive peak Current (kA)	Negative peak Current (kA)	Positive peak Current (kA)	Negative peak Current (kA)
No FCL	29 %	31.2 %	24.6 %	23.1 %
SDBR	16.3 %	17.6 %	19.4 %	18.3 %

In the above section, we have discussed several points for showing the superiority of the BFCL over no FCL and SDBR centered protection framework. At the very beginning, We have discussed the condition of real and reactive power where reactive power is seen very close to zero unless the fault condition and active power is in good condition which indicates that our system is in is working perfectly. Next, from the reference tracking section we have seen how the simulated power is following the reference power. After that, by applying 3LG and 2LG fault in no FCL, SDBR and the proposed BFCL system

we have observed the fault current limiting performance of BFCL over other two typical method. For more clarification of visualization the graphical representation is also shown using RMS values of fault current limitation and in numerical tabular form. Finally, by showing the percentage of improvement comparatively for BFCL over other two classical method it is clear that BFCL performance is much superior than those.

CHAPTER 7

CONCLUSION AND FUTURE WORK

In this work, a solid state bridge type fault current limiter based protection scheme for the IBDG system has been proposed. The background and impacts of short circuit fault has been studied, an overview of fault current limiter has also been presented. Design and control strategy of bridge type fault current limiter has been discussed in details. We have designed the control system of the IBDG system for the proper integration of the BFCL with the system. We simulate the system in MATLAB/Simulink. The behaviour of bridge type fault current limiter and the controllers during simulation has been studied. For this, current and voltage across bridge type fault current limiter elements such as IGBT, diodes, shunt branch are checked and discussed in details. Input, output and other variables that plays important role for the controller has also been discussed. From this, we assured that the proposed system behaves as our expectation. Balanced and unbalanced short circuit faults have been applied to examine the behaviour of the proposed protection scheme during short circuit fault and it holds it's position well. Faults were simulated for 0.08 seconds. System response during the fault is well. One of the major concerns of other fault current protection measures is: not being able to limit fault current at the first cycle of the fault which is devastating for the system. But it has been shown that the proposed system can limit the fault current at the very beginning of the first cycle of the fault current.

The proposed protection scheme for inverter based distributed generation system with BFCL and the proposed control system performs well. The proposed strategy reduces the fault current almost 30 % compared to no protection and 15 to 20 % over SDBR based protection scheme. Reference power as well as voltage is tracked well with the proposed protection scheme.

Future work

The primary reason of choosing a solid state fault current limiter is the cost over SFCL. Although SSFCLs have some advantages such as fast switching, no need for recovery time hence they have the theoretical ability of withstanding consecutive faults but SSFCLs are not so reliable as SFCLs. In fact SSFCLs have high failure rate. Steady state

loss is another problem of all SSFCLs. “**Fig. 7.1**” shows the leakage current flow through the shunt branch of bridge type fault current limiter during normal steady state operation. Theoretically, there should be no voltage and current in the shunt branch during steady state operation, but from the figure it has been clearly demonstrated that there are both voltage and current in the shunt branch which increases the system loss. So, there are

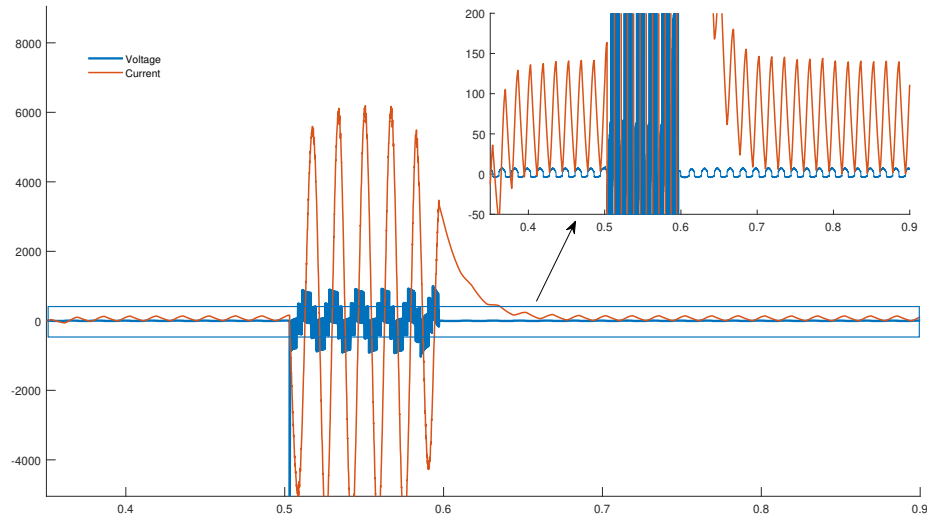


Figure 7.1 Leakage voltage & current in the shunt branch of BFCL

potential scopes of improvement in the internal design of bridge type fault current limiter to make the steady state operation lossless or to reduce the loss at a good extent. Although semiconductor devices plays the key role for this steady state loss but further studies are required to make improvement in this case and to make SSFCLs more reliable. Details feasibility studies are also required for the practical implementation and commercialization of most of the SSFCLs including BFCL.

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