

**International Islamic University Chittagong**  
**Department of Computer Science & Engineering**  
*B. Sc. in CSE Semester Final Examination, Autumn 2024*  
**Course Code: CSE 3521 Course Title: Computer Architecture**  
 Total marks: 50 Time: 2.5 hours

[Answer all the questions. Figures in the right hand margin indicate full marks. -M: Marks, C:CLO, D: Domain]

M C D

**Group-A**

- |           |   |   |   |   |
|-----------|---|---|---|---|
| 1. a)     | Compare the performance of single-cycle, multi-cycle, and pipeline processors in terms of CPI. Discuss with a detailed example.   | 5 | 5 | 1 |
| <b>OR</b> |   |   |   |   |
|           | Suppose you are given an instruction add \$s1,\$t3,\$t4. Describe the complete operation of the datapath using the instruction with a figure.   |   |   |   |
| b)        | Explain the structural differences between single and multi-cycle data path.  | 5 | 5 | 2 |
| <b>OR</b> |   |   |   |   |
|           | What temporary registers are used in multicycle datapath? What changes are required for the multiplexer in multicycle datapath?   |   |   |   |
| 2. a)     | Differentiate the single and multi-cycle data path on the basis of their control signal.  | 5 | 5 | 2 |
| b)        | A program has the following instruction mix: 30% ALU operations, 25% loads, 10% stores, 30% branches, and 5% jumps. If each instruction type has the following cycle counts: ALU - 1, Load - 2, Store - 2, Branch - 1, Jump - 1, calculate the overall CPI. | 5 | 2 | 3 |

**Group-B**

- |           |  |   |   |   |
|-----------|--|---|---|---|
| 3. a)     | What is the role of control hazards in pipeline architecture? Propose a method to minimize control hazards.  | 5 | 5 | 2 |
| b)        | Design a diagram showing the working of a branch instruction in a pipelined data path and explain the steps involved.  | 5 | 5 | 2 |
| 4. a)     | Define <i>miss penalty</i> , <i>cache miss</i> , <i>hit rate</i> , <i>tag</i> in caching, memory hierarchy   | 5 | 3 | 2 |
| b)        | What is DMA controller? Describe the configuration of DMA controller.  | 5 | 3 | 3 |
| 5. a)     | What is TLB? Discuss the operation of paging and TLB using flow diagram?   | 5 | 3 | 2 |
| b)        | Explain the direct mapped cache system with figure.  | 5 | 4 | 3 |
| <b>OR</b> |  |   |   |   |
| a)        | Explain the role of virtual memory in modern computer systems. Describe the translation process of virtual addresses to physical addresses with the help of a diagram. | 5 | 3 | 2 |
| b)        | What is RAID? Explain at least three of its type with example.   | 5 | 4 | 3 |