International Islamic University Chittagong (IIUC)

Department of Electronic and Telecommunication Engineering

Final Exam

Program: B.Sc (Engg.) **Semester: Autumn2022**

Course Code: ETE-4827/4847 **Course Title: VLSI System Design & Modeling**

Total Marks: 50 **Time: 2.5Hours**

[(i) Answer all the questions. The figures in the right-hand margin indicate full marks.]

[(ii) Course Learning Outcomes (COs) and Bloom's Levels are mentioned in additional Columns.]

Course Outcomes (COs) of the Questions	
CLO1	Identify and understanding the basic knowledge of VLSI technology and Circuit.
CLO2	Recognize and illustrate the theoretical knowledge of MOS circuit device design and fabrication.
CLO3	Apply and Analyze the knowledge to design different sequential and combinational login circuit using NMOS, PMOS and CMOS.

Bloom's Levels of the Questions						
Letter Symbols	**R**	**U**	**Ap**	**An**	**E**	**C**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

Group A

Q1.	(a)	Explain Ion implementation process and Describe the Ion implementation set up with proper diagram.	05	CLO2	An
	(b)	Explain the thermal oxidation and distinguish between dry and wet oxidation.	05	CLO2	U,An
		OR			
Q1.	(c)	Describe the step by step n-MOS fabrication process with diagram.	05	CLO2	An
	(d)	Describe thestep by step n-well CMOS fabricationprocess with necessary diagram.	05	CLO2	U, An
Q2.	(a)	Sketch the NMOS AND andNAND Gate. Also describe their operation with switching characteristics.	05	CLO3	Ap
	(b)	Sketch the PMOS OR and NOR Gate. Also describe their operation with switching characteristics.	05	CLO3	Ap

Group B

Q3.	(a)	Design a CMOS Full adder circuit and sketch the stick diagram.	10	CLO3	C
		OR			
Q3.	(b)	Design a 4×1 multiplexer using CMOS and pass transistor.	10	CLO3	C
Q4.	(a)	Discuss the field programmable gate array (FPGA) chip implementation design style.	05	CLO2	An
	(b)	Discuss the standard cell based design style for CMOS implementation.	05	CLO2	An
Q5.	(a)	Write the advantages of HDL based design technique and explain the importance of Verilog HDL.	05	CLO2	An
	(b)	Write a program for 2×1 MUX using RTL Verilog code and structural code.	05	CLO3	C