International Islamic University Chittagong (IIUC)

Department of Electronic and Telecommunication Engineering

Semester End Examination

Program: B.Sc. (Engg.) | **Semester: Spring 2025**
Course Code: ETE-1245 | **Course Title: Basic Electronics**
Total Marks: 50 | **Time-2.5 Hours**

[(i) Answer all the questions. The figures in the right-hand margin indicate full marks.]

[(ii) Course Learning Outcomes (COs) and Bloom's Levels are mentioned in additional Columns.]

Course Learning Outcomes (CLOs)of the Questions	
CLO1	Apply knowledge of Basic Electronics to Distinguish schematic symbol and Recognize basic concepts of electronic components and circuits.
CLO2	To analyze the functionality of various devices including several types of Diode, BJT and FET through problem analysis.

Bloom's Levels of the Questions						
Letter Symbols	**R**	**U**	**Ap**	**An**	**E**	**C**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

PART-A

Q1.a)	With neat sketch, explain the operation of PNP transistor for both forward and reverse bias junction.	5	An	**CLO1**
b)	Discuss the major difference between BJT and JFET. Sketch the basic construction of n channel and p channel JFET.	5	An	**CLO1**
Q2.a)	Explain the physical reason of Emitter Biasing providing more stability than Fixed Biasing of BJT.	5	U	**CLO1**
b)	Determine R_C, R_E, and R_B for Emitter Bias Configuration of BJT when $I_c = 0.5I_{C(Sat)}$, $I_{C(Sat)} = 8mA$, $V_{CC} = 18$ V, and $\beta = 110$. [Symbols in the question carry usual meanings]	5	Ap	**CLO2**

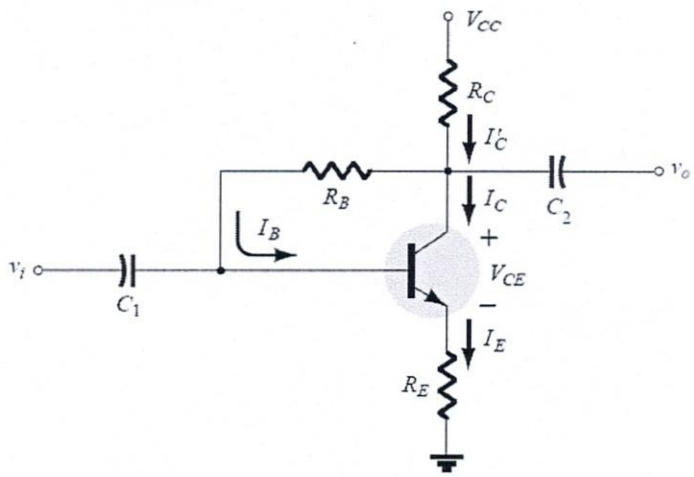

Fig. 1

OR

Q2.a) Evaluate following for the fixed-bias configuration of Fig. 2. 5 E **CLO2**
(i) I_{BQ} and I_{CQ} (ii) V_{CEQ} (iii) V_B and V_C (iv) V_{BC}. (v) $I_{csat.}$

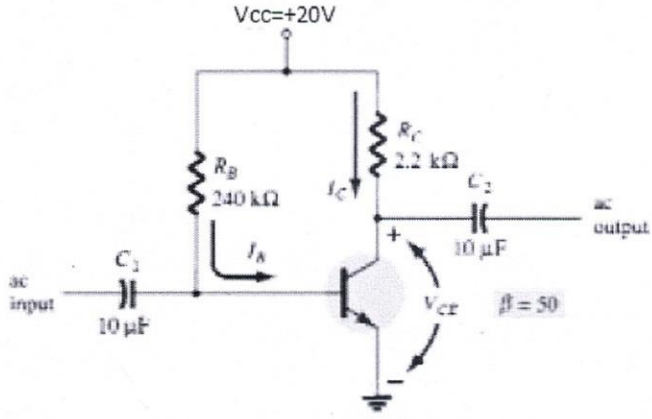

Fig:2

b) Estimate For the emitter bias network of Fig. 3 (i) I_B (ii) I_C (iii) V_{CE} (iv) V_C (v) V_E (vi) V_B (vii) V_{BC}. 5 E **CLO2**

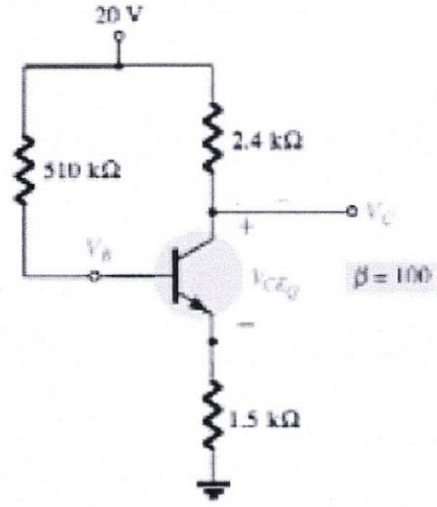

Fig:3

PART-B

Q3.a) Compare and contrast between JFET and MOSFET. 5 An **CLO1**
b) Explain the operation and construction of a Depletion type MOSFET. 5 An **CLO1**

Q4. For the self-bias configuration of Fig. 4 10 C **CLO2**
(i) Sketch the transfer curve for the device.
(ii) Superimpose the network equation on the same graph.
(iii) Estimate I_{DQ} and V_{GSQ}.
(iv) Evaluate V_{DS}, V_D, V_G, and V_S.

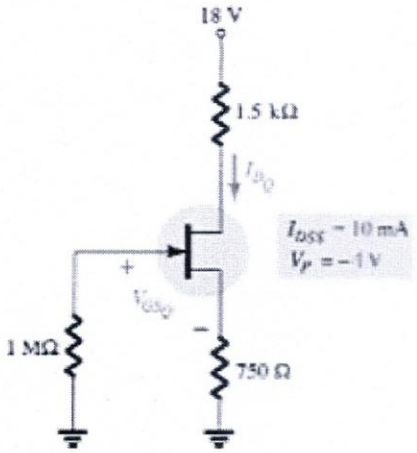

Fig: 4

Q5.a)	For a common base configuration r_e transistor model show that $Z_i=r_e$, $Z_0=\infty\Omega$, $A_v=R_L/r_e$ and $A_i=-1$	5	An	**CLO2**
b)	For a common-base configuration of Fig. 5 with I_E=4 mA, α =0.98, and an ac signal of 2 mV applied between the base and emitter terminals: (i) Estimate the input impedance. (ii) Point out the voltage gain if a load of 0.56 k Ωis connected to the output terminals. (iii) Evaluate the output impedance and current gain.	5	C	**CLO2**

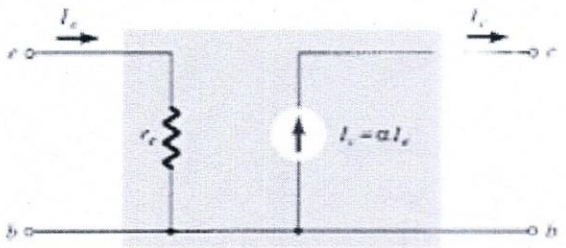

Fig.5

OR

Q5.a)	Determine the following for the network of Fig. 6. (i) I_D and V_{GS}. (ii) V_D.	5	An	**CLO2**

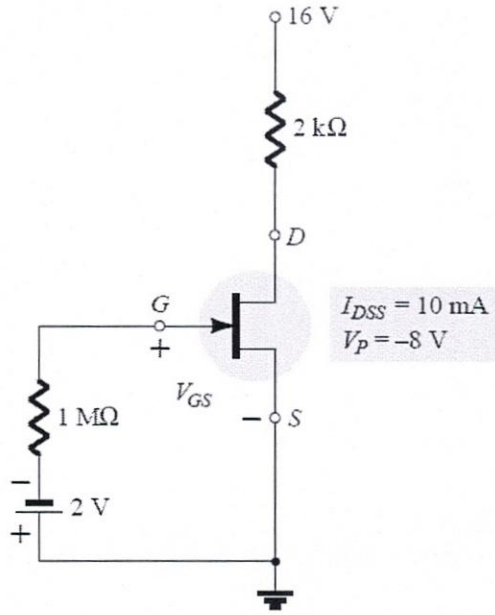

Fig.6

(b) Consider the Circuit Diagram in Fig. 7. Determine: 5 An **CLO2**

(i) I_D and V_{GS} (ii) V_D(iii) V_S (iv) V_{DS} (v) V_{DG}

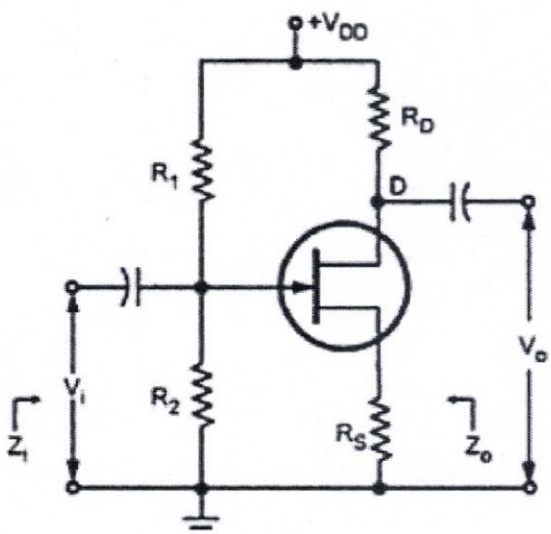

Fig. 7

Where, V_{DD} = 22V, R_1 = 2.1 MΩ, R_2 = 270 kΩ, R_D = 2.4 kΩ, R_E = 1.5 kΩ, I_{DSS} = $V_{DD}/2$ and V_P = - ($V_{DD}/4$) V