International Islamic University Chittagong
Department of Electrical and Electronic Engineering

Final Examination Autumn-2018 | Program: B.Sc. Engg. (EEE)
Course Code: EEE 4711 | Course Title: VLSI System Design and Modeling Technique
Time: 2 hours 30 minutes | Full Marks: 50

Part A

[Answer any ***two*** questions from the followings; f ll marks.]

1(a). Explain CMOS fabrication technique using n-well process. 4
1(b). How IC's are made? Describe Czochralski process for single crystal growth with proper diagram. 6

2(a). Write short note on ...ample des... les and micron rules.
2(b). In intra ... ...te down the following rules (minimum width and sepa...
(a) ...olysilicon (c) Metal 1
2(c). Draw a ... explain a layout d... am of a CMOS inverter using lambda based design rules. 4

3(a). What is etchin... Explain about wet and dry etching. 4
3(b). Explain PM... brication process step by step. 5
3(c). What is wa... 1

Part B

[Answer any ***three*** questions from the followings; figures in the right margin indicate full marks.]

4(a). What is pass transistor? Sketch following expression using static CMOS: 1+4
i. $\overline{ABC.(D+E)}$
ii. $\overline{(AF + \overline{\ ^{?} + DE).F}}$
4(b). What is dynamic ... Explain the operation of dynam...

5(a). Classify Simple programmable logi... (SPDL). Explain each of them with example. 7
5(b). What is stick diagram? Draw a 2-input NOR gate using stick diagram. 3

6(a). Discuss about VHDL terms. Also explain about "entity". 6
6(b). What is FPGA? Explain. Also mention the advantages and disadvantages of FPGA. 4

7(a). Sketch two input X-OR and X-NOR gate using static CMOS gate. 4
7(b). Explain Full custom and semi-custom design with example. 4
7(c). What is tristate buffer? Write down its truth table. 2