International Islamic University Chittagong
Department of Electrical and Electronic Engineering

Final Examination Autumn-2020	Program: B.Sc. Engg. (EEE)
Course Code: **EEE-4753**	Course Title: **VLSI-I**
Time: **5 hours** (Writing -**4 hours 30 minutes** + **30 minutes** submission time)	Full Marks: **50** (**Written** 30 + **Viva**/**Viva-Quiz**-20)

[Answer **each of the** questions from the followings; Figures in the right margin indicate full marks. **Answer script must be submitted through online method within 5 hours from starting time. Also, write down the Q. Set on the front page of your answer script]**

Q. Set-2

1(a).	"Explain NMOS fabrication steps in detail with your own words. Also, differentiate between the process of NMOS and PMOS fabrication.	**CO1**	**E**	**04**
1(b).	Differentiate between n-Well and p-Well CMOS technology.	**CO1**	**U**	**02**
2(a).	Design and explain the layout diagram of a 5-input CMOS NOR gate using lambda-based design rules.	**CO3**	**C**	**05**
2(b).	Differentiate between scalable design rules and micron rules.	**CO1**	**U**	**01**
3.	Design a static CMOS gate computing - (i) $Y= \overline{(AB).(C+D+E)+FG+HI+J(K+L+M)}$ (ii) $Y= \overline{(A+B).C+D+EFG+H+I+J(K+L+M)}$	**CO2**	**C**	**06**
4(a).	Make a comparative analysis among Full-custom design, Semi- custom design and Programmable Logic Array.	**CO1**	**E**	**02**
4(b).	What is stick diagram? Design a 6-input OR gate using stick diagram with explaining the stick diagram rules.	**CO3**	**R, C**	**04**
5(a).	"In VHDL, designers can use the type system to write much more structured code", Justify it.	**CO1**	**E**	**04**
5(b).	Implement the following expression using PAL. $Y= \overline{A}BC+A\overline{B}C+AB\overline{C}+\overline{A}BC$	**CO3**	**C**	**02**
6.	Viva/Viva-Quiz: The time of viva/viva-quiz will be declared in google classroom.	**CO1**	**U**	**20**