## **International Islamic University Chittagong Department of Electrical and Electronic Engineering**

Final Examination Autumn-2020	Program: B.Sc. Engg. (EEE)
Course Code: EEE-4753	Course Title: VLSI-I
Time: 5 hours (Writing -4 hours 30	Full Marks: <b>50</b> (Written 30 + Viva/Viva-Quiz-20)
minutes + 30 minutes submission time)	

[Answer each of the questions from the followings; Figures in the right margin indicate full marks. Answer script must be submitted through online method within 5 hours from starting time. Also, write down the Q. Set on the front page of your answer script]

	Q. Set-1			
1(a).	"Doping levels and doping uniformity in selected areas of the surface of the wafer can be accurately controlled by ion implantation process"-justify it with explaining the operation of an ion implantation arrangement.	CO1	Е	03
1(b).	Explain PMOS fabrication steps in detail with your own words. Also, differentiate between the process of NMOS and PMOS fabrication.	CO1	U	03
2(a).	Design and explain the layout diagram of a 6-input CMOS AND gate using lambda-based design rules.	CO3	С	05
<b>2(b).</b>	Differentiate between scalable design rules and micron rules.	CO1	U	01
3.	Design a static CMOS gate computing -  (i) $Y = \overline{(A+B)(C+D+EF+G+HI+J)(K+L+M)}$ (ii) $Y = \overline{(ABC+D+E+FG+H+IJ(K+L+M))}$	CO2	С	06
4(a).	Make a comparative analysis among Full-custom design, Semi- custom design and Programmable Logic Array.	CO1	E	02
<b>4(b).</b>	What is stick diagram? Design a 4-input NOR gate using stick diagram with explaining the stick diagram rules.	CO3	R, C	04
5(a).	Compare the system verilog and VHDL code that illustrate the behavioral descriptions of a module computing a random Boolean function,	CO3	E	04
5(b).	Y= ABC+ABC+ABC Implement the following expression using PAL.	CO3	С	02
	$Y = \overline{A}BC + A\overline{B}C + A\overline{B}C + \overline{A}BC$		-	
6.	Viva/Viva-Quiz: The time of viva/viva-quiz will be declared in google classroom.	CO1	U	20