International Islamic University Chittagong
Department of Electrical and Electronic Engineering

Final Assessment Test Autumn-2020	Program: B.Sc. Engg. (EEE)
Course Code: **EEE-2407**	Course Title: **Digital Electronics**
Time: **5 hours** (Writing - **4 hours 30 minutes** + **30 minutes** submission time)	Full Marks: **50** (**Written** 30 + **Viva/Viva-Quiz**-20)

[Answer each of the questions **(1-5)** from the followings; Figures in the right margin indicate full marks.**]**

SET-B

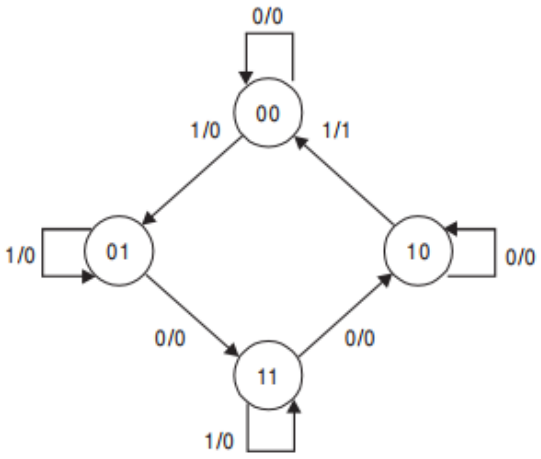
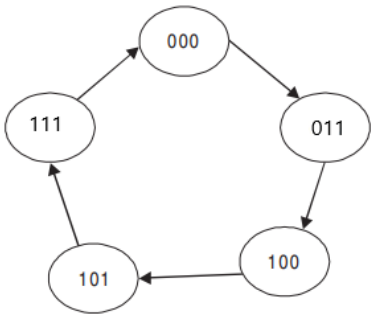
1(a)	Design a combinational circuit that compares two 3bit numbers A&B to check if A is greater than B. The circuit output is equal to one if the all bits of A is greater than all bits of B and zero otherwise.	**CO3**	**C**	**03**
1(b)	Explain the procedure to reduce the carry propagation delay in 4 bit binary parallel adder.	**CO3**	**E**	**03**
2(a).	Implement the Function F(A,B,C) = ABC′+A′BC′+ABC+AB′C′ using a 3×8 decoder.	**CO3**	**Ap**	**02**
2(b).	Implement the 3-variable function F (A,B,C) = A′B+ ABC′+ABC using a 4-to-1 multiplexer.	**CO3**	**Ap**	**02**
2(c)	Design Decimal to BCD encoder circuit.	**CO3**	**C**	**02**
3(a).	Design a sequential circuit using J-K flip flop. The state diagram is given in Fig.1.  Fig.1	**CO2**	**C**	**04**
3(b).	Find the reduced state table and draw the reduced state diagram by reducing the number of states in Table1.	**CO2**	**R**	**02**

	Table1-State table <table><tr><th rowspan="2">Present State</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr><tr><th>x=0</th><th>x=1</th><th>x=0</th><th>x=1</th></tr><tr><td>a</td><td>d</td><td>a</td><td>0</td><td>0</td></tr><tr><td>b</td><td>e</td><td>a</td><td>0</td><td>0</td></tr><tr><td>c</td><td>g</td><td>f</td><td>0</td><td>1</td></tr><tr><td>d</td><td>a</td><td>d</td><td>1</td><td>0</td></tr><tr><td>e</td><td>a</td><td>d</td><td>1</td><td>0</td></tr><tr><td>f</td><td>c</td><td>b</td><td>0</td><td>0</td></tr><tr><td>g</td><td>a</td><td>e</td><td>1</td><td>0</td></tr></table>			
4(a)	Design a synchronous counter using T Flip-flop whose state diagram is shown in Fig.2.  Fig.2	**CO3**	**C**	**03**
4(b).	Design a MOD-5 asynchronous down counter.	**CO3**	**C**	**02**
4(c).	Compare between synchronous counter and asynchronous counter.	**CO3**	**An**	**01**
5(a).	Design a serial in parallel out and a parallel in serial out register to store the data 11100 & 10100.	**CO3**	**C**	**03**
5(b).	Design a 7-bit Johnson Counter and a 5-bit Ring Counter.	**CO3**	**C**	**03**
6.	Viva/Viva-Quiz: The time of viva/viva-quiz will be declared in Google classroom.			**20**