# International Islamic University Chittagong Department of Electrical and Electronic Engineering 

Final Assessment Test Autumn- Program: B.Sc. Engg. (EEE)

## 2020

Course Code: EEE-2407
Time: $\mathbf{5}$ hours (Writing $\mathbf{4}$ hours
$\mathbf{3 0}$ minutes $\mathbf{} \mathbf{3 0}$ minutes
submission time)

## Course Title: Digital Electronics

Full Marks: 50 (Written 30 + Viva/Viva-Quiz-20)
[Answer each of the questions (1-5) from the followings; Figures in the right margin indicate full

> marks.]
> SET-A

1(a). Design a circuit of octal to binary encoder with the following information.
(i) MNPQXY are the $1^{\text {st }}$ to $6^{\text {th }}$ digits of your student ID. If your first digit $M$ is 1 then assume it as $D_{1}$, similar explanation is true for other cases.
(ii) Expression for output variables $\mathrm{x}, \mathrm{y}$ and z are, $\mathrm{x}=\mathrm{M}$ (write is as $\mathrm{D}_{1}$ (for example) as explained earlier $)+\mathrm{N}+\mathrm{P}+\mathrm{Q}, \mathrm{y}=\mathrm{N}+\mathrm{P}+\mathrm{Q}+\mathrm{X}, \mathrm{z}=\mathrm{P}+\mathrm{Q}+\mathrm{X}+\mathrm{Y}$.
1(b). Implement a Boolean function $F(A, B, C)=\sum(M, N, X, Y)$ by multiplexer, where $\mathrm{M}, \mathrm{N}, \mathrm{X}$ and Y are the $3^{\text {rd }}$ to $6^{\text {th }}$ digits of your student ID, respectively.

2(a). Develop a full adder circuit using a decoder and two OR gates. Choose, $\mathrm{S}=\sum(\mathrm{M}, \mathrm{N}, \mathrm{X}, \mathrm{Y})$ and $\mathrm{C}=\sum(\mathrm{P}, \mathrm{Q}, \mathrm{X}, \mathrm{Y})$, where, MNPQXY are the $1^{\text {st }}$ to $6^{\text {th }}$ digits of your student ID.
2(b). Design a combinational circuit by using PLA, where, $\mathrm{F}_{1}=\mathrm{A}^{\prime} \mathrm{B}+\mathrm{AC}^{\prime}$ and $\mathrm{F}_{2}=\mathrm{AC}+\mathrm{B}^{\prime} \mathrm{C}$.

3(a). Explain the stepwise logic diagram and timing relationship of CO1 C 03 master-slave flip-flop using RS flip-flop.
3(b). Identify the steps of state reduction process towards reducing the $\mathbf{C O 2}$ An 03 states of the following state diagram.


Fig. 3(b): State diagram
4(a). Design a counter that has a repeated sequence of six states (starting $\quad \mathbf{C O 3} \quad \mathrm{C} \quad 03$
from 000 and end state is 110 ).
4(b). Suppose, $\mathrm{N}=\mathrm{Y}+1$ is the number of flip-flop, where Y is the last digit of your student ID (If Y=0 with your student ID, at that case choose your $2^{\text {nd }}$ last digit as Y , if both the last digits are 0 , then choose $\mathrm{Y}=2$ ). Calculate the mod number and design a mod counter with the calculated mod number using J-K flip-flop.

5(a). Compare among various types of data shifting process.
5(b). From your study, give your comments on the difference in construction and timing sequence of 4 -bit and 5-bit Johnson counter.
6. Viva/Viva-Quiz: The time of viva/viva-quiz will be declared in google classroom.

CO3 E
03

CO1, U,

