International Islamic University Chittagong

Dept. of Computer Science & Engineering (CSE)

B.Sc. in CSE, Semester Final Examination, Spring 2018

Course Code: CSE 2305 **Title:** Digital Logic Design

Total Marks: 50 Time: 2 hours 30 Minutes

Group - A

1. a. Define parallel adder. Design a 4-bit parallel adder with the solution of carry propagation problem. 5

   b. A combinational circuit is defined by the following three Boolean functions: 5

$$F_1 = (X + Y)' + XYZ$$
$$F_2 = (X + Z)' + X'YZ$$
$$F_1 = XY'Z + (X + Z)'$$

   Design the circuit with a decoder and external OR gates.

2. a. i. Design a 16-to-1 multiplexer using 4-to-1 multiplexers only. 5

   ii. Using two 2-to-4 decoders, design a logic circuit to realize the following Boolean function

   $F(A,B,C) = \Sigma(0, 1, 4, 6, 7)$.

   b. Design a combinational circuit that compare two 4-bit numbers A and B to check if they are equal. The circuit has one output x, so that x=1 if A=B and x=0 if A is not equal to B. 5

3. a. How does *JK* flip-flop remove the indeterminate states of *S-R* flip-flop? Design a *JK* flip-flop and show its characteristic equation, characteristic table, logic diagram and timing diagram. 5

   b. What is flip-flop triggering problem? Describe the master-slave JK flip-flop with timing diagram. 5

Group-B

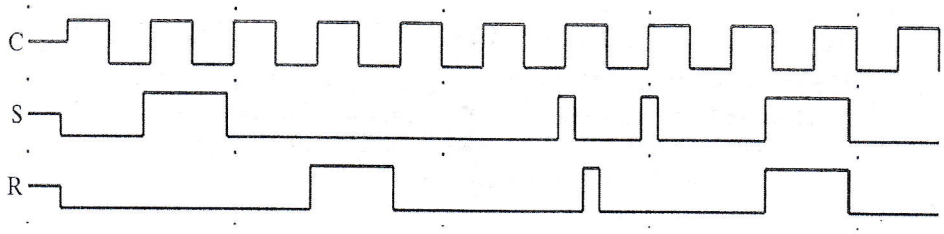
4. a. Consider a 128x8 ROM. How many address and words are consisted in this ROM. Specify the each word size in bit. Design a ROM with AND-OR-INVERT gates with the following function: 5

$$F(X, Y) = \sum(2, 4, 5)$$
$$F(X, Y) = \sum(1, 5, 7)$$

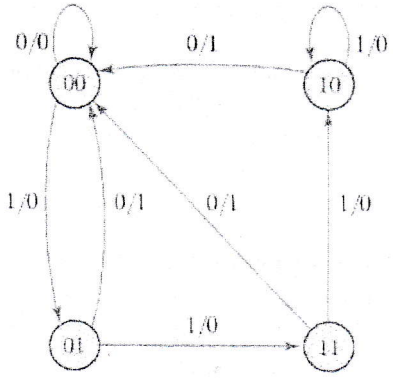
   b. If the present (ABC) state is 110, and the input X=0; what will be the next state if the flip flops input functions are as follows: 5

$$JA = B'X \qquad KA = 1$$
$$JB = A + C'X' \qquad KB = XC' + CX'$$
$$JC = AX + A'B'X' \qquad KC = X$$

5. a. Describe the behavior of master-slave flip-flop with respect to the following timing diagrams. 5



b. Define the state diagram and state equation. 5



From the above state diagram derived the

i. State table
ii. Excitation table
iii. State equations

6. a. Design a 4-bit asynchronous counter with *JK* flip-flops and explain its operation with timing diagram 5

b. Design a *3-bit* Up-Down counter with *T* flip-flop. 5

7. a. Define register. Draw the memory logic diagram. Construct a RAM for 4 word of 5 bit each. 5

b. Design a sequential circuit described by the following state equations using JK flip-flops. 5

$$A(t+1) = xAB + yA'C + xy$$
$$B(t+1) = xAC + y'BC'$$
$$C(t+1) = x'B + yAB'$$