International Islamic University Chittagong
Department of Electrical and Electronic Engineering
B. Sc. Engineering in EEE
Midterm Examination, Autumn 2022

Course Code: **EEE 4753** Course Title: **VLSI I**

Time: 1 hour 30 minutes Full Marks: 30

(i) Answer all the questions. The figures in the right-hand margin indicate full marks.

(ii) Course Outcomes (COs) and Bloom's Levels are mentioned in additional Columns.

Course Outcomes (COs) of the Questions	
CLO1	Reflect a basic understanding of IC design and fabrication technique.
CLO2	Solve different problems related to MOS Device, CMOS logic circuits and Fabrication.
CLO3	Design and development of different CMOS logic circuits.

Bloom's Levels of the Questions						
Letter Symbols	**R**	**U**	**Ap**	**An**	**E**	**C**
Meaning	Remember	Understand	Apply	Analyze	Evaluate	Create

1.	a)	'MOS technology is superior to Bipolar technology and within MOS technology, CMOS technology is adopted as the design medium for VLSI'- Justify the statement with analytical examples.	**CO1**	**An**	**3+2**
1.	b)	Suppose two customers wanted same digital design from you. The first customer gave you a very short amount of time and the second customer gave you a long period of time as the only condition for designing. i. What design approach should be adopted for the first customer? State the reason. ii. What design approach should be adopted for the second customer? State the reason. iii. Describe the full design procedure of the design approach adopted for the second customer, from beginning to last.	**CO1**	**An , U**	**1+1 +3**
2.	a)	Derive I-V characteristic equation of PMOS transistor for resistive and saturation region. Also verify from those equations that drain current I_D is linear and constant for resistive and saturation region. Why we use three types of I_D equation when studying MOSFET? What would be the possible problem if we use only one I_D?	**CO2**	**E**	**5**
2.	b)	For a MOSFET with W/L = 2, V_t= 0.6V, calculate – (a) The values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current I_{DS} = 200μA. (b) The value of V_{GS} required to cause the device to operate as a 400Ω resistor for very small V_{DS}. Consider that $K_n = (\varepsilon\mu_n/D)$ = **196 μA/V^2.**All the symbols have their usual meanings.	**CO2**	**Ap**	**5**

Or,

2) a)	Derive the drain current equation for the NMOS devices in three different regions and also draw and describe the input and output characteristics curve of NMOS using the equations.	**CO2**	**E**	**3+2**
2) b)	Considering **Fig.1**. Calculate I_D, V_{DS}, and verify the assumed bias state of below transistor for $V_{tp} = -0.4$ V, $K_p = 60\ \mu A/V^2$, and $W/L = 2$. Where symbols have their usual meaning.	**CO2**	**Ap**	**5**

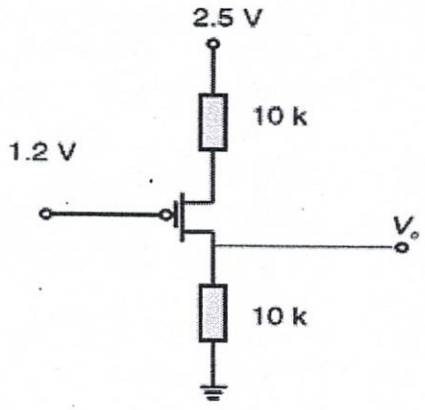

Fig.1.

3) a)	Draw a CMOS inverter and explain its operation (with your own words) with transfer characteristic curve and show different state of both transistors at different input voltage. Also show the state for which drain current ID will be maximum.	**CO1**	**C**	**5**
3) b)	"Noise margin is the amount of ratio that a CMOS circuit could withstand without compromising the operation of circuit"- Is it right or wrong? Write down your logical arguments with necessary figures and expressions.	**CO2**	**An**	**5**