International Islamic University Chittagong
Department of Electrical and Electronic Engineering

Final Examination Autumn-2018 | Program: B.Sc. Engg. (EEE)
Course Code: EEE-2407 | Course Title: Digital Electronics
Time: 2 hours 30 minutes | Full Marks: 50

Part A

[Answer any ***two*** questions from the followings; figures in the right margin indicate full marks.]

1(a). Design a circuit that compares two 2-bit numbers, A and B, to check whether they are equal or unequal. The circuit has three output x,y,z, so that x=1 if A=B or y=1 if A>B or z=1 if A<B. 3

1(b). Explain the main functional difference between a Binary adder and BCD adder with an example. 1

1(c). Design a BCD adder to add two single digit decimal numbers. Your answer should include the detail design procedure. 6

2(a). Design a 4-bit binary parallel adder including look ahead carry generator. 5

2(b). Define decoder. Implement a full-subtractor circuit by means of a decoder. 3

2(c). Construct a 5×32 decoder using two 4×16 decoders. 2

3(a). Design a Quadruple 2-to-1 line multiplexer. 4

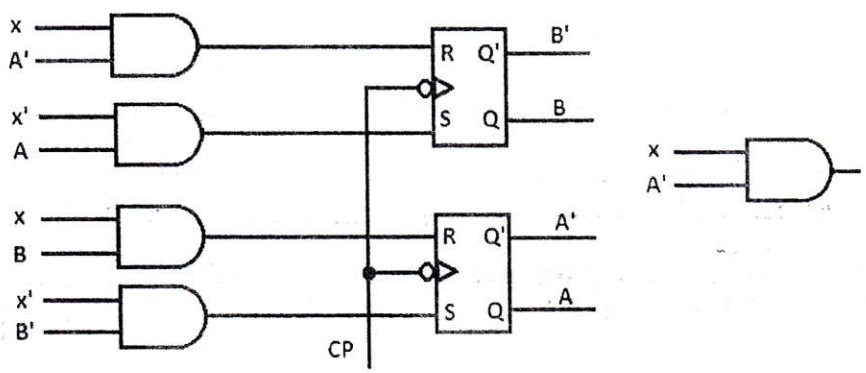
3(b). Draw the characteristic and excitation tables of RS and JK flip flops. 3

3(c). Draw the logic diagram of a 'D' & 'T' flip flop using only NAND gates. 3

Part B

[Answer any ***three*** questions from the followings; figures in the right margin indicate full marks.]

4(a). Draw the state table and state diagram for the following sequential circuit. 6



4(b). Design a 3-bit synchronous counter using D flipflop. 4

5(a). How two NOR gates can construct a 1-bit memory element? Explain with proper logic diagram. 2

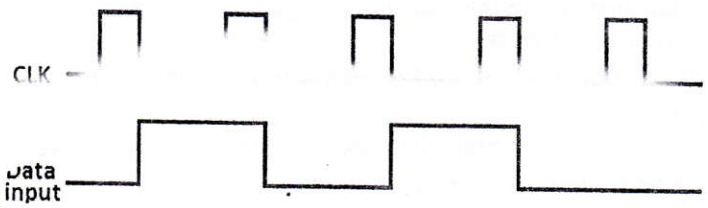
5(b). Draw the logic diagram of a JK flip-flop and find out the next state of the flip-flop for the following conditions explaining the operation of the circuit. 4

i) Present state Q(t)=0, Inputs J=1 and K=0.

ii) Present state Q(t)=1, Inputs J=1, K=1.

5(c). Introduce the multiple transition problem in triggering of clocked flip-flops. How this problem can be solved by using a master-slave flip-flop? 4

6(a). Draw a 4-bit serial in/serial out shift register. Also draw the output wave forms for the following data input and the clock waveform if it is fed to the above register. 5



6(b). Assume you need to store 8-bit of data in a register. How many clock pulse you will need to load the data and to read the date if the register is a: 2

(i) Serial in-serial out register

(ii) Serial in-parallel out register

(iii) Parallel in-serial out register

(iv) Parallel in-parallel out register

6(c). Draw the sequence table of a 5-bit Jonson counter and its logic diagram. 2

7(a). De[illegible] serial out shift register. 3

7(b). R[illegible]uce the states of the following state table and draw the reduced state table and diagram. 4

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	d	1	0
b	e	d	0	0
c	a	b	0	1
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

7(c). Draw the state table for a 3 bit counter and determine the flip-flop inputs if it is to be designed with J-K flip-flop. 3